1995

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Monolithic finite gain amplifiers employing active voltage attenuators in the feedback and a charge conserving macromodel for MOSFETs

by

Joon-Yub Kim

A Dissertation Submitted to the

Graduate Faculty in Partial Fulfillment of the

Requirements for the Degree of

DOCTOR OF PHILOSOPHY

Department: Electrical and Computer Engineering
Major: Electrical Engineering (Microelectronics)

Approved:

Signature was redacted for privacy.

In Charge of Major Work

Signature was redacted for privacy.

For the Major Department

Signature was redacted for privacy.

For the Graduate College

Iowa State University
Ames, Iowa
1995

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A	amplitude of v_1 or v_I (0-P)
A'	amplitude of v_I' (0-P)
A_{Di}	area of drain of M_i, i=1, 2, 3, 4
A_{opt}	optimum amplitude (0-P) for maximum signal to non-signal output ratio
A_{Si}	area of source of M_i, i=1, 2, 3, 4
B	amplitude of v_2 (0-P)
C_{BC}	bulk-channel capacitance
C_{BCi}	junction capacitance of D_{BCi}, i=1,...,n
C_{BCiJO}	zero bias junction capacitance of D_{BCi}, i=1,...,n
C_{BDi}	bulk-drain junction capacitance of M_i, i=1, 2, 3, 4
C_{BDJ}	bulk-drain junction capacitance
C_{BSi}	bulk-source junction capacitance of M_i, i=1, 2, 3, 4
C_{BSJ}	bulk-source junction capacitance
C_C	compensation capacitance for infinite bandwidth
C_{gbo}	gate-bulk overlap capacitance per unit channel length
C_{GC}	gate-channel capacitance
C_{GCi}	gate-channel capacitance of M_i, i=1,...,n
C_{GDi}	gate-drain overlap capacitance of M_i, i=1, 2, 3, 4
C_{GDO}	gate-drain overlap capacitance
C_{gdo}	gate-drain overlap capacitance per unit channel width
C_{GSi}	gate-source overlap capacitance of M_i, i=1, 2, 3, 4

C_{GSP}	parasitic capacitance in experimental set-up between gate and source nodes
C_{GSO}	gate-source overlap capacitance
C_h	holding capacitor in sampling and hold circuit
C_J	zero bias bottom junction capacitance density
C_{JSW}	zero bias sidewall junction capacitance density
C_{OV}	gate-source/gate-drain overlap capacitance per unit channel width
C_{OX}	gate oxide capacitance
C_{ox}	gate oxide capacitance density
C_{OXi}	gate oxide capacitance in macromodel, i=1,...,n
C_S	capacitance between source node and ground
D_{BC}	diode between bulk and channel
D_{BCi}	diode between bulk and channel in macromodel, i=1,...,n
D_{BDJb}	diode between bulk and drain for bottom junction in macromodel
D_{BDJs}	diode between bulk and drain for sidewall junction in macromodel
D_{BSJb}	diode between bulk and source for bottom junction in macromodel
D_{BSJs}	diode between bulk and source for sidewall junction in macromodel
DW	channel width reduction
E	electron energy
F_N	Fermi level in n-type semiconductor
F_P	Fermi level in p-type semiconductor
F	ac transfer function
f	frequency
f_1	lower limit of noise band
f_2	upper limit of noise band
g_{dsi}	output conductance of M_i, i=1, 2, 3, 4
g_{mbi}	bulk-channel transconductance of M_i, i=1, 2, 3, 4
g_{mi}	gate-channel transconductance of M_i, i=1, 2, 3, 4

I_{Di}	drain current of M_i, i=1, 2, 3, 4
I_{DiQ}	operating point drain current of M_i, i=1, 2, 3, 4
i_N	total output noise current
i_{Ni}	output noise current of M_i, i=1, 2, 3, 4
I_{Di}	drain current of M_i, i=1, 2, 3, 4
I_S	substrate junction saturation current
k	Boltzmann's constant
K_f	Flicker noise coefficient
K'	transconductance parameter
$K'_{modified}$	modified transconductance parameter by mobility degradation
L	channel length
Lambda	channel length modulation parameter
L_D	lateral diffusion length
L_{drawn}	drawn channel length
L_i	channel length of M_i, i=1, 2, 3, 4
L_{max}	maximum allowed channel length
L_{min}	minimum allowed channel length
$L_{2,opt}$	optimum length for L_2
M_i	MOSFET, i=1, 2, 3, 4,....,n+1
MJ	bulk bottom junction grading coefficient
MJSW	bulk sidewall junction grading coefficient
N_{fs}	fast surface-state density
N_{sub}	substrate doping concentration
P_d	power dissipation
P_{Di}	perimeter of drain of M_i, i=1, 2, 3, 4
P_{Si}	perimeter of source of M_i, i=1, 2, 3, 4
q	electron charge
Q_{Ci}	channel charge of M_i, i=1,...,n+1

R_G	resistance of resistor connected to gate
R_S	source resistance
S_I	total noise current spectral density
S_{Ii}	noise current spectral density of M_i, i=1, 2, 3, 4
S_{ITi}	thermal noise current spectral density of M_i, i=1, 2, 3, 4
S_{Ifi}	flicker noise current spectral density of M_i, i=1, 2, 3, 4
T	absolute temperature in Kelvin
T_{OX}	gate oxide thickness
t	time
$UCRIT$	critical field for mobility degradation
$UEXP$	critical field exponent in mobility degradation
V_{adj}	voltage source in macromodel
V_B	voltage at the gate of M_2 in Attenuator II and summing attenuator
v_B	ac component of V_B
V_{BB}	voltage at the gate of M_4 of summing attenuator
V_{BSi}	bulk-source voltage of M_i, i=1, 2, 3, 4
V_{BQ}	dc operating voltage of V_B
V_{BSi}	bulk-source voltage of M_i, i=1, 2, 3, 4
V_{CBi}	channel-bulk voltage of M_i, i=1,...,n+1
V_D	drain voltage
V_{DD}	power supply voltage
V_{DSi}	drain-source voltage of M_i, i=1, 2, 3, 4
V_{FB}	flat band voltage
V_G	gate voltage
V_G'	output voltage of pulse generator
V_{GB}	gate-bulk voltage
V_{GCi}	gate-channel voltage of M_i, i=1,...,n+1
V_{GOFF}	gate voltage in off-state

V_{GON}	gate voltage in on-state
V_{GSi}	gate-source voltage of M_i, i=1, 2, 3, 4
V_h	voltage across C_h
$V_{h,f}$	voltage across C_h in off period
V_I	input voltage
v_I	ac component of V_I
V_i	voltage of input i, i=1, 2, 3, 4
v_i	ac component of V_i, i=1, 2, 3, 4
V_I'	input voltage of amplifier
v_I'	ac component of V_I'
V_{IQ}	dc operating voltage of V_I
V_{iQ}	dc operating voltage of V_i
V_{IQ}'	dc operating voltage of V_I'
V_{max}	maximum drift velocity of carriers
v_{NO}	output noise voltage
V_O	output voltage
v_O	ac component of V_O
V_O'	output voltage of amplifier
v_O'	ac component of V_O'
V_{OA}	output voltage of summing amplifier
V_{OB}	output voltage of subtracting amplifier
V_{OQ}	dc operating voltage of V_O
V_{OQ}'	dc operating voltage of V_O'
V_S	source voltage
V_{SB}	source-bulk voltage
V_{Ti}	threshold voltage of M_i, i=1, 2, 3, 4
V_{Th}	threshold voltage
V_{T0}	zero-bias threshold voltage

$V_{TO,practical}$	zero-bias threshold voltage of practical MOSFET
V_{TON}	zero-bias threshold voltage of n-channel MOSFET
V_+	non-inverting input voltage of operational amplifier
V_-	inverting input voltage of operational amplifier
W	channel width
W_i	channel width of M_i, i=1, 2, 3, 4
W_{drawn}	drawn channel width
W_{max}	maximum allowed channel width
W_{min}	minimum allowed channel width
X_J	metallurgical junction depth
XQC	coefficient for share of channel charge attributed to drain
$\tilde{\alpha}$	dc transfer function of attenuator
$\tilde{\alpha}_i$	dc transfer function of summing attenuator for input i, i=1, 2
$\tilde{\alpha}_S$	dc transfer function of attenuator of summing attenuator
α	small signal attenuation factor of attenuator
α_i	small signal attenuation factor of summing attenuator for input i, i=1, 2
α_{jk}	small signal attenuation factor, j=1, 2, 3, f; k=1, 2, 3
ϵ_{OX}	dielectric constant of SiO_2
γ	bulk threshold parameter
ϕ	strong inversion surface potential
ϕ_B	bulk junction built-in potential
μ_0	surface mobility
ω_i	angular frequency of v_i, i=1, 2
ω	angular frequency of v_I or v_I'

ACKNOWLEDGMENTS

I would like to express my heartful thanks to my advisor, Dr. Randall L. Geiger. I can never thank him enough for his cordial guidance, encouragement, and support during my Ph.D. study at Iowa State University. His technical excellence and foresight have been of great support to me and have had an important effect on my life.

I would like to thank Drs. Hsung-Cheng Hsieh, Marwan Hassoun, Sachin Sapatnekar, and Carl J. Bern for serving as my graduate committee and for sharing their busy schedules to help me with my research. Dr. Hassoun is appreciated especially for his sincere help whenever I needed him to fabricate the chips for my research.

I also appreciate Dr. Richard K. Hester of Texas Instruments Inc. for his valuable discussions and comments on my research, and Drs. Robert J. Weber and Gary Tuttle for their kind help when I needed to use their equipment.

I would like to thank Dr. Richard E. Horton for giving me the opportunity to work as a TA. Without the financial support that he helped to provide, I would have had financial difficulties during my Ph.D. study.

I cannot thank my parents, brother, and sisters enough for their endless love and support in every respect. I believe I am always encouraged and feel rich whenever I remember my parents are always there for me. Their strength, good-will, honesty, and love have guided my life.

It is impossible to thank my wife enough, Jin-Ok, who was always beside me with all kinds of support and love. I am so lucky to have such a wonderful wife. Thank you to my daughter, Jee-Sun, and my son, Jacob. They make me always happy and proud.

CHAPTER 1. INTRODUCTION

This dissertation presents two separate topics which both support the development of the analog and mixed signal integrated circuit design field. The first topic concentrates on a new way of realizing versatile linear finite gain amplifiers for monolithic applications and the second is directed to the development of a macromodel for MOSFETs, that is specifically useful for the simulation of non-ideal charge injection effects of MOSFET switches. The two topics are presented in separate chapters in this dissertation. Each chapter has a full organization including introduction, main body, and conclusion.

In discrete circuits, designers have an easy and convenient way for the realization of linear precision finite gain voltage amplifiers [1-6]. This is done by employing a linear precision voltage attenuator in the feedback path of an operational amplifier or a large forward gain amplifier. The linear precision voltage attenuator in the feedback path can be easily realized by combining two or more precision discrete resistors. A precision discrete resistor is very easy to make, but it is difficult and inconvenient to make one with a sufficiently large resistance in integrated form. Thus, a practical way for making precise and practical continuous-time finite gain amplifiers has eluded designers for many years.

The first topic in Chapter 2 is the result of attempts to solve this problem inherent to integrated circuits [7-12]. Three MOS active voltage attenuators useful for the realization of finite gain amplifiers in monolithic circuits are presented. The attenuators are two single-input attenuators and a summing attenuator that has two inputs or multiple

inputs. The summing attenuator is derived from one of the single-input attenuators. The attenuators are very simple in structure consisting of only MOSFETs. They are easy to fabricate in standard semiconductor processes. The attenuation factor of the attenuators ideally depends only upon the ratios of the dimensions of the MOSFETs making it possible to precisely control the attenuation factor over a wide range of gains. In Chapter 2, the attenuators and the versatile finite gain amplifiers realized with the attenuators along with operational amplifiers are introduced. An analysis along with the simulated performance of the attenuators and amplifiers are presented. Design methods for minimum noise and for minimum power dissipation are discussed. The attenuators and amplifiers are characterized by experimentally measuring the accuracy of the gain, the range of the linear region, and the harmonic and intermodulation distortions.

One major cause of the degradation in performance of analog and mixed-signal integrated circuits utilizing MOSFET switches is the disturbances to the adjacent nodes when they are turned off [13-31]. Widely used in analog and mixed signal integrated circuits, a MOSFET switch injects unwanted channel charge to adjacent capacitors while it is turned off. The overlap capacitance between the gate and the drain/source also couples with the capacitance of the adjacent nodes and pushes or pulls the adjacent node voltages as the gate voltage changes. These errors, which MOSFET switches induce, are an inherent limitation present in designing precision analog and mixed signal integrated circuits utilizing MOSFET switches.

In Chapter 3, a charge conserving macromodel for MOSFETs is introduced. This macromodel provides a convenient and effective tool for analyzing and resolving the charge injection problem [32, 33]. The macromodel for MOSFETs can be used to simulate both dc and ac characteristics of MOSFETs, but it is especially useful in the simulation of the charge injection effect of MOSFET switches. The macromodel can be

used directly in standard circuit simulators such as SPICE. In Chapter 3, qualitative review of the semiconductor physics related in the MOS structure is discussed. Based on this review, the structure of the macromodel are introduced. Principles and strategies for the implementation of the macromodel are explained. The macromodel is compared with the MOSFET models in SPICE. The accuracy of the macromodel is verified by comparing the simulation results using the macromodel with experimental measurement results for a simple sample-and-hold circuit.

CHAPTER 2. MONOLITHIC FINITE GAIN AMPLIFIERS EMPLOYING ACTIVE VOLTAGE ATTENUATORS IN THE FEEDBACK

2.1 Introduction

Finite gain amplifiers with exactly controlled gain, high linearity, and low output noise find extensive applications in both integrated and discrete circuits. In discrete circuits, the easiest and most popular way to construct a finite gain amplifier is to use an operational amplifier (op-amp) and a voltage attenuator in the feedback loop [1-6]. Here, a voltage divider, consisting of two resistors connected in a series, has been used in discrete circuits for the voltage attenuator. This approach to building a finite gain amplifier does not extend practically to integrated circuits because realization of resistors of exact and large resistance and good performance are very inefficient. In general, resistors in integrated circuits require large areas, consume too much power, have parasitic capacitances, and are difficult to be realized with exact resistance values to be attractive in many applications such as the voltage attenuators.

Thus, to realize finite gain amplifiers in integrated circuits as easily as in discrete circuits, we need an alternative voltage attenuator which has a good performance when it is realized in integrated circuits. Voltage attenuators find applications in data converters and in the input stages of transconductance amplifiers as well as in feedback amplifiers. Some research has been done on monolithic attenuators [34-36]. Van Horn proposed a

simple active voltage attenuator structure consisting of two MOSFETs [34], Loh investigated its dynamic range performance [35], and Qin developed a multiple output voltage attenuator based on Van Horn's single output attenuator structure [36]. These attenuators exhibit attractive performances such as a precisely controllable attenuation ratio, high linearity, low noise, and high input impedance. To obtain a good performance, the attenuators in these investigations were limited to the case where the MOSFETs in the voltage attenuators were placed in individual wells. Unfortunately, these active voltage attenuators have a fundamental drawback. They have a substantial deterministic offset voltage. This drawback makes the attenuators applicable to only special cases where the dc operating voltage of the output is not required to be controlled. Furthermore, extensions into a multiple input voltage attenuator structure necessary to realize summing or subtracting amplifiers with two or more inputs have not been proposed nor appear to be readily attainable.

In this chapter, efforts are focused on finding practical and useful monolithic voltage attenuators [7-12]. The analysis and performance of an active voltage attenuator consisting of two MOSFETs fabricated in a common substrate, an extension of the original two MOSFET attenuator introduced by Van Horn [34], are presented. Then, a second version of the voltage attenuator is introduced which overcomes the offset adjustability problem of the first version and is expandable to a multiple input voltage attenuator structure. The extension of the second attenuator into a multiple input attenuator structure is finally introduced, focusing on the two input summing attenuator. After the characterization of each attenuator, the characterization of a finite gain amplifier employing each attenuator is presented. It will be demonstrated that the versatility, performance, and simplicity of the set of voltage attenuators make them useful. Hence, employing the attenuators with op-amps, practical monolithic finite gain amplifiers can be

realized as easily as in discrete circuits. The performance of the attenuators and amplifiers are characterized with experiments by measuring the accuracy of gain, the range of linear region, and the degree of linearity.

2.2 Attenuator I and Finite Gain Amplifier Employing It

The analyses of the active voltage attenuator originally introduced by Van Horn covered only the operation principle and noise characteristics. These analyses were limited to the simple case where the substrate of each of the two MOSFETs was separated into individual wells [34-36].

In this section, a detailed characterization of the active attenuator using two cascaded MOSFETs (the Van Horn attenuator) fabricated in a common substrate is presented. The common substrate attenuator offers several advantages. First, both n-channel and p-channel attenuators can be monolithically fabricated in a standard CMOS process. Second, the required area for the attenuator is smaller. Third, the parasitic junction capacitance at the boundary of the separate well for each transistor does not exist.

The operation principle, harmonic distortion analysis, random noise analysis, frequency response analysis, design, and performance of the attenuator, including power consumption and size consideration, are investigated. The harmonic distortion analysis and the random noise analysis of an amplifier using the attenuator in the feedback loop of an op-amp are also investigated. The performance of the attenuator and the amplifier employing the attenuator in the feedback loop of an op-amp is experimentally characterized by measuring the accuracy of the small signal gain, the dc transfer characteristic which shows the range of the linear region, and the harmonic and intermodulation distortions which show the degree of linearity.

2.2.1 Operation principle of Attenuator I

An active linear voltage attenuator (Attenuator I) consisting of two n-channel MOSFETs is shown in Fig. 2.1. The substrate is common for both MOSFETs and is connected to the source of the lower MOSFET, M1. The circuit operates as a linear voltage attenuator when M1 is in the ohmic region and M2 is in the saturation region. Assuming the zero bias threshold voltage of both MOSFETs is V_{TON}, the operating conditions will be met provided

$$V_{TON} < V_I < V_{DD} + V_{T2} \,, \tag{2.1}$$

where

$$V_{T2} = V_{TON} + \gamma\left(\sqrt{\phi + V_O} - \sqrt{\phi}\right) . \tag{2.2}$$

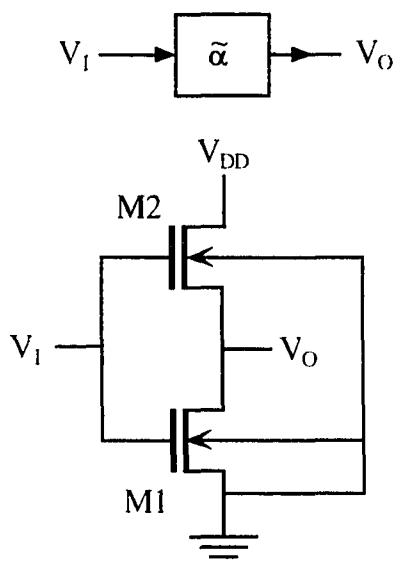


Figure 2.1: Circuit and block diagram of Attenuator I consisting of two n-channel MOSFETs

Since M1 is operating in the ohmic region and M2 in the saturation region, from the square law model for the MOSFETs, the drain current of each MOSFET is given by

$$I_{D1} = K'\frac{W_1}{L_1}\left(V_I - V_{TON} - \frac{V_O}{2}\right)V_O \tag{2.3}$$

and

$$I_{D2} = K'\frac{W_2}{2L_2}(V_I - V_{T2} - V_O)^2. \tag{2.4}$$

Equating the two drain currents from (2.3) and (2.4), the implicit relationship between V_I and V_O of Attenuator I is obtained as

$$2R\left(V_I - V_{TON} - \frac{V_O}{2}\right)V_O = \left\{V_I - V_{TON} - V_O - \gamma\left(\sqrt{\phi + V_O} - \sqrt{\phi}\right)\right\}^2, \tag{2.5}$$

where

$$R = \frac{W_1/L_1}{W_2/L_2}. \tag{2.6}$$

If each MOSFET in the attenuator is fabricated in a separate substrate and the substrate of each MOSFET is connected to its source, the dc transfer characteristic relating V_I and V_O becomes a linear equation,

$$V_O = \tilde{\alpha}(V_I) = \alpha(V_I - V_{TON}) \tag{2.7}$$

where α is the small signal attenuation factor of the attenuator. In this case, α is

$$\alpha = 1 - \sqrt{\frac{R}{R+1}} = 1 - \sqrt{\frac{W_1/L_1}{W_1/L_1 + W_2/L_2}}. \tag{2.8}$$

Equation (2.7) is a special case of (2.5), which reduces to (2.7) when the bulk effect term in (2.5) is ignored. When the substrate is separate, the small signal attenuation factor given by (2.8) is precisely determined by width/length ratios. If the substrate is common, the relationship between the input and output is still nearly linear, but the linearity is somewhat obscured by the implicit relationship between V_O and V_I as shown in (2.5).

The dc transfer characteristics between V_I and V_O as calculated from (2.5) and (2.7) for R=1 are shown in Fig. 2.2. The values in Table 2.1 are used for ϕ, V_{TON}, and γ which are standard for a 2μm p-well CMOS process. Note, when the substrate is common, the dc transfer characteristic of the attenuator given by (2.5) is also very linear, as shown in Fig. 2.2, even though the equation is seemingly nonlinear.

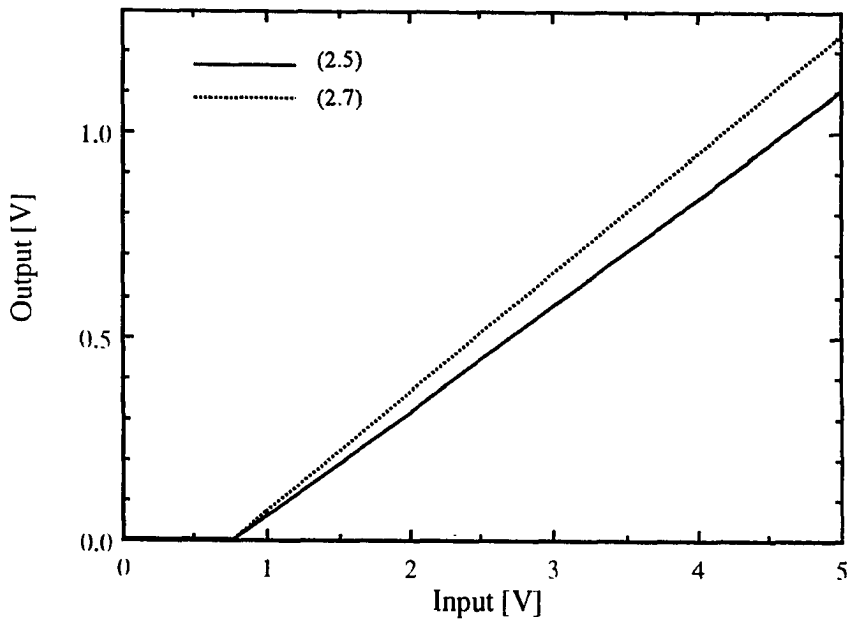


Figure 2.2: dc transfer characteristics of Attenuator I

Table 2.1: Parameter set

parameter	value	parameter	value
V_{TON}	0.777 V	C_J	8.252×10^{-5} F/m^2
γ	0.5255 V$^{1/2}$	MJ	0.6394
ϕ	0.6 V	C_{JSW}	5.806×10^{-10} F/m
K'	5.663×10^{-5} A/V^2	$MJSW$	0.2010
C_{ox}	8.125×10^{-4} F/m^2	L_D	0.25 μm
K_f	3×10^{-24} V^{2}F	ϕ_B	0.8 V

To test the dependence of the small signal attenuation factor on the process parameters, SPICE simulations using the level 1 model were performed. The small signal attenuation factor is the slope of the dc transfer function at a dc operating point. The small signal attenuation factor of the same attenuator, for which the dc transfer function is shown in Fig. 2.2, was simulated at an input dc operating voltage of 3V. When ϕ is increased by 10% from the value given in Table 2.1, the small signal attenuation factor increases by 0.267% and when ϕ is decreased by 10%, it decreases by 0.289%. When V_{TON} is increased by 10% from the value given in Table 2.1, the small signal attenuation factor decreases by 0.0911% and when V_{TON} is decreased by 10%, it increases by 0.0888%. When γ is increased by 10% from the value given in Table 2.1, the small signal attenuation factor decreases by 1.06% and when γ is decreased by 10%, it increases by 1.08%.

2.2.2 Harmonic analysis of Attenuator I

In order to analyze the small signal attenuation factor and the harmonic distortion for the common substrate case, the dc transfer characteristic given by (2.5) is expanded into Taylor's series. For the input of $V_I=V_{IQ}+v_I$, the output, V_O, is expanded as

$$V_O = \tilde{\alpha}(V_I) = V_{OQ} + \left(\frac{dV_O}{dV_I}\right)_Q v_I + \frac{1}{2}\left(\frac{d^2V_O}{dV_I^2}\right)_Q v_I^2 + \ldots \tag{2.9}$$

where Q denotes the dc operating point. $V_{OQ} = \tilde{\alpha}(V_{IQ})$ is given from (2.5).

$$\left(\frac{dV_O}{dV_I}\right)_Q = \alpha$$

$$= \frac{-RV_{OQ} + \left\{V_{IQ} - V_{TON} - V_{OQ} - \gamma\left(\sqrt{\phi + V_{OQ}} - \sqrt{\phi}\right)\right\}}{R\left(V_{IQ} - V_{TON} - V_{OQ}\right) + \left\{V_{IQ} - V_{TON} - V_{OQ} - \gamma\left(\sqrt{\phi + V_{OQ}} - \sqrt{\phi}\right)\right\}\left(1 + \frac{\gamma}{2\sqrt{\phi + V_{OQ}}}\right)}, \tag{2.10}$$

and

$$\left(\frac{d^2V_O}{dV_I^2}\right)_Q$$

$$= \frac{R\alpha(\alpha-2)\left\langle 1+\alpha\left[\alpha\left(1+\frac{\gamma}{2\sqrt{\phi+V_{OQ}}}\right)^2 - 2 - \frac{\gamma}{\sqrt{\phi+V_{OQ}}} + \left\{V_{IQ}-V_{TON}-V_{OQ}-\gamma\left(\sqrt{\phi+V_{OQ}}-\sqrt{\phi}\right)\right\}\frac{\gamma}{4\left(\phi+V_{OQ}\right)^{\frac{3}{2}}}\right]\right\rangle}{R\left(V_{IQ}-V_{TON}-V_{OQ}\right) + \left\{V_{IQ}-V_{TON}-V_{OQ}-\gamma\left(\sqrt{\phi+V_{OQ}}-\sqrt{\phi}\right)\right\}\left(1+\frac{\gamma}{2\sqrt{\phi+V_{OQ}}}\right)} \tag{2.11}$$

α, defined by (2.8) and (2.10), is the small signal attenuation factor of the attenuator for the separate substrate case and for the common substrate case, respectively. Equation (2.8) is a special case of (2.10) when the bulk effect terms in (2.10) are ignored, and (2.8) clearly shows that the small signal attenuation factor can be controlled over a wide range by controlling the dimensions of the MOSFETs in the attenuator. This is also true in the case of a common substrate, even though it is obscured by the complicated expression for the attenuation factor for the common substrate case as given by (2.10).

If $v_I = A\sin\omega t$, then, taking only the first three terms in (2.9), we obtain

$$V_O \cong h_0 + h_1 \sin\omega t + h_2 \cos 2\omega t \ , \tag{2.12}$$

where

$$h_0 = V_{OQ} + \frac{1}{4}\left(\frac{d^2V_O}{dV_I{}^2}\right)_Q A^2 , \tag{2.13}$$

$$h_1 = \left(\frac{dV_O}{dV_I}\right)_Q A = \alpha A , \tag{2.14}$$

and

$$h_2 = -\frac{1}{4}\left(\frac{d^2V_O}{dV_I{}^2}\right)_Q A^2 . \tag{2.15}$$

In these expressions, h_0 is the total dc, h_1 is the "desired" ac signal, and h_2 is the 2nd harmonic distortion component of the attenuator output. Note that the 2nd-order distortion introduces additional dc offset as shown in (2.13), which will generally be very small. Using (2.5), and (2.10), the small signal attenuation factor, α, and the output dc operating voltage, V_{OQ}, for given R and V_{IQ}, or the necessary R and the output dc operating voltage, V_{OQ}, for given α, and V_{IQ} can be calculated. Then, using (2.10), (2.11), (2.14) and (2.15), the signal output, h_1, and the 2nd harmonic distortion of the output, h_2, can be calculated for a given input signal amplitude.

2.2.3 Noise analysis of Attenuator I

A noise equivalent circuit of Attenuator I, based on noiseless MOSFETs and output noise current sources, and its equivalent small signal circuit are shown in Fig. 2.3. At a given dc operating point,

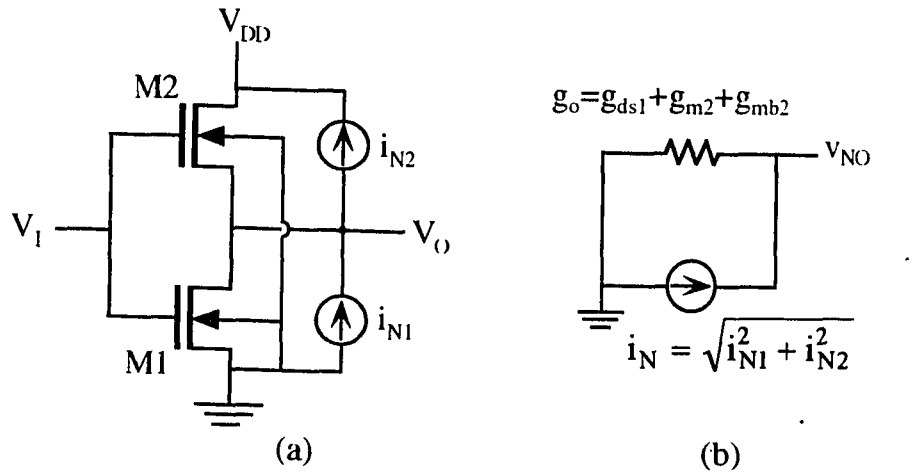


Figure 2.3: (a) Noise equivalent circuit of Attenuator I based on noiseless transistors and output noise current sources, (b) noise small signal equivalent circuit

$$g_{ds1} = \left(\frac{\partial I_{D1}}{\partial V_{DS1}}\right)_Q = K'\frac{W_1}{L_1}\left(V_{IQ} - V_{TON} - V_{OQ}\right), \tag{2.16}$$

$$g_{m2} = \left(\frac{\partial I_{D2}}{\partial V_{GS2}}\right)_Q = K'\frac{W_2}{L_2}\left\{V_{IQ} - V_{TON} - V_{OQ} - \gamma\left(\sqrt{\phi + V_{OQ}} - \sqrt{\phi}\right)\right\}, \tag{2.17}$$

and

$$g_{mb2} = \left(\frac{\partial I_{D2}}{\partial V_{BS2}}\right)_Q = g_{m2}\frac{\gamma}{2\sqrt{\phi + V_{OQ}}}. \tag{2.18}$$

The total output conductance, g_o, is defined by

$$g_o = g_{ds1} + g_{m2} + g_{mb2}. \tag{2.19}$$

Since M1 is operating in the ohmic region and M2 is operating in the saturation region, for the output noise sources the respective noise current spectral density for each MOSFET is given by

$$S_{I1} = S_{IT1} + S_{If1} = 4kTg_{ds1} + \frac{2K_f K' I_{D1Q}}{C_{OX} L_1^2 f} , \tag{2.20}$$

and

$$S_{I2} = S_{IT2} + S_{If2} = \frac{8}{3} kTg_{m2} + \frac{2K_f K' I_{D2Q}}{C_{OX} L_2^2 f} , \tag{2.21}$$

including the thermal noise and the flicker noise. The total noise current spectral density of the attenuator is defined by

$$S_I = S_{I1} + S_{I2} . \tag{2.22}$$

From Fig. 2.3 (b), the output noise voltage(rms) in the frequency band $f_1 \le f \le f_2$ is given by

$$v_{NO} = \frac{i_N}{g_o} = \frac{\sqrt{i_{N1}^2 + i_{N2}^2}}{g_o} = \frac{\sqrt{\int_{f_1}^{f_2} S_I df}}{g_o} . \tag{2.23}$$

Thus, from (2.16)-(2.23),

$$v_{NO} = \left[\frac{L_2}{W_2} \left\{ M + N \left(\frac{1}{L_1^2} + \frac{1}{L_2^2} \right) \right\} \right]^{\frac{1}{2}} , \tag{2.24}$$

where M and N are given by

$$M = \frac{R\left(V_{IQ} - V_{TON} - V_{OQ}\right) \frac{4kT}{K'} (f_2 - f_1) + \left\{ V_{IQ} - V_{TON} - V_{OQ} - \gamma \left(\sqrt{\phi + V_{OQ}} - \sqrt{\phi} \right) \right\} \frac{8kT}{3K'} (f_2 - f_1)}{\left[R\left(V_{IQ} - V_{TON} - V_{OQ}\right) + \left\{ V_{IQ} - V_{TON} - V_{OQ} - \gamma \left(\sqrt{\phi + V_{OQ}} - \sqrt{\phi} \right) \right\} \left(1 + \frac{\gamma}{2\sqrt{\phi + V_{OQ}}} \right) \right]^2} \tag{2.25}$$

and

$$N = \frac{R\left(V_{IQ} - V_{TON} - \frac{V_{OQ}}{2}\right)V_{OQ}\frac{2K_f}{C_{OX}}\ln\frac{f_2}{f_1}}{\left[R\left(V_{IQ} - V_{TON} - V_{OQ}\right) + \left\{V_{IQ} - V_{TON} - V_{OQ} - \gamma\left(\sqrt{\phi + V_{OQ}} - \sqrt{\phi}\right)\right\}\left(1 + \frac{\gamma}{2\sqrt{\phi + V_{OQ}}}\right)\right]^2} \quad (2.26)$$

Using (2.6) and (2.24)-(2.26), the output noise voltage(rms) can be calculated for a given dc operating point, W_1, L_1, W_2, L_2, a noise frequency band, and temperature.

2.2.4 Frequency response analysis of Attenuator I

Figure 2.4 shows the small signal equivalent circuit of the attenuator and its reduced equivalent circuit for the case of common substrate. The parasitic capacitances involved can be modeled as

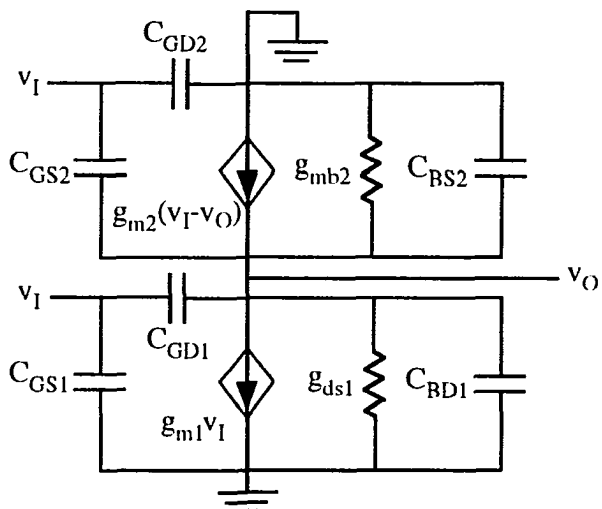
$$C_{GD1} = C_{OX}W_1L_D + \frac{1}{2}W_1L_1C_{OX}\ , \quad (2.27)$$

$$C_{BD1} = \frac{C_JA_{D1}}{\left[1 + \frac{V_{OQ}}{\phi_B}\right]^{MJ}} + \frac{C_{JSW}P_{D1}}{\left[1 + \frac{V_{OQ}}{\phi_B}\right]^{MJSW}} + \frac{1}{2}\frac{C_JW_1L_1}{\left[1 + \frac{V_{OQ}}{\phi}\right]^{\frac{1}{2}}}\ , \quad (2.28)$$

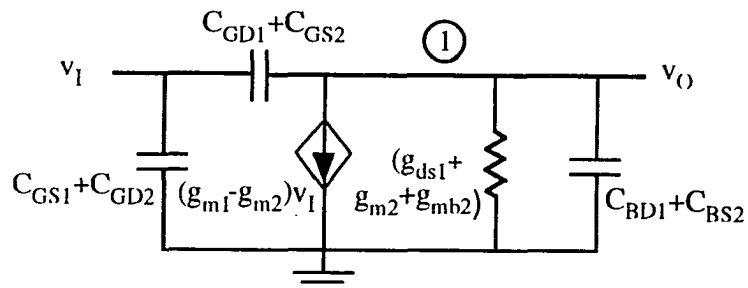
$$C_{BS2} = \frac{C_JA_{S2}}{\left[1 + \frac{V_{OQ}}{\phi_B}\right]^{MJ}} + \frac{C_{JSW}P_{S2}}{\left[1 + \frac{V_{OQ}}{\phi_B}\right]^{MJSW}} + \frac{2}{3}\frac{C_JW_2L_2}{\left[1 + \frac{V_{OQ}}{\phi}\right]^{\frac{1}{2}}}\ , \quad (2.29)$$

and

$$C_{GS2} = C_{OX}W_2L_D + \frac{2}{3}W_2L_2C_{OX}\ . \quad (2.30)$$



(a)



(b)

Figure 2.4: Small signal equivalent circuits

Solving the node equation at node 1 in Fig. 2.4 (b), the small signal transfer function is obtained as

$$\frac{v_O(s)}{v_I(s)} \equiv F(s) = \frac{-g_1 + sC_1}{g_o + s(C_1 + C_2)} , \tag{2.31}$$

where g_o is given by (2.19),

$$g_1 = g_{m1} - g_{m2} , \tag{2.32}$$

$$C_1 = C_{GD1} + C_{GS2} , \tag{2.33}$$

$$C_2 = C_{BD1} + C_{BS2} , \tag{2.34}$$

and, from (2.3),

$$g_{m1} = \left(\frac{\partial I_{D1}}{\partial V_{GS1}}\right)_Q = K' \frac{W_1}{L_1} V_{OQ} . \tag{2.35}$$

When the substrate is separate, g_{mb2} is zero, and C_{BD2} is involved in place of C_{BS2}. Thus, C_{BS2} in (2.34) and in Fig. 2.4 should be replaced by C_{BD2}, where

$$C_{BD2} = \frac{C_J A_{D2}}{\left[1 + \frac{V_{DD} - V_{OQ}}{\phi_B}\right]^{MJ}} + \frac{C_{JSW} P_{D2}}{\left[1 + \frac{V_{DD} - V_{OQ}}{\phi_B}\right]^{MJSW}} . \tag{2.36}$$

From (2.31), note g_1 is negative, the small signal transfer function of Attenuator I has a pole and a zero in the left half plane of the complex plane. Because both the zero and pole are in the left half plane, it is possible to cancel the pole and zero such that the frequency response has an infinite bandwidth by adding a capacitor to the attenuator. From the calculations of (2.31) and Fig. 2.4, the pole and zero in the small signal transfer function cancel when a capacitor given by

$$C_C = \left(\frac{1}{\alpha} - 1\right) C_1 - C_2 \tag{2.37}$$

is connected to Attenuator I between the output node and the ground.

If we want to have an attenuator of α=0.1 at V_{IQ}=3V, (2.5) and (2.10) require R=3.992 and V_{OQ}=0.2214V for the common substrate case. If we pick W_1=2μm and L_1=2.505μm for M1 and W_2=2μm L_2=10μm satisfying (2.6), the 3dB bandwidth simulated with the above model and the parameter values in Table 2.1 is 138Mhz. The drain and source diffusion areas were assumed to be 2μmx4μm for M1 and 2μmx4μm for M2. If we want to have an infinite bandwidth, we can add a capacitor of 0.1079pF between the output terminal and ground.

2.2.5 Analysis of finite gain amplifier employing Attenuator I

In this section, an amplifier formed with an op-amp and Attenuator I in the feedback loop as shown in Fig. 2.5 is considered. Assuming the op-amp is ideal,

$$V_I' = V_O = \tilde{\alpha}(V_I) = \tilde{\alpha}(V_O'), \tag{2.38}$$

or

$$V_O' = \tilde{\alpha}^{-1}(V_I'), \tag{2.39}$$

that is, the dc transfer function of the amplifier is the inverse function of the dc transfer function of the attenuator in the feedback loop. Thus, the transfer function between the input, V_I', and the output, V_O', of the amplifier is given by (2.5), when V_O is replaced by V_I' and V_I by V_O'.

If the substrate is separate, the dc transfer function of the amplifier is given by,

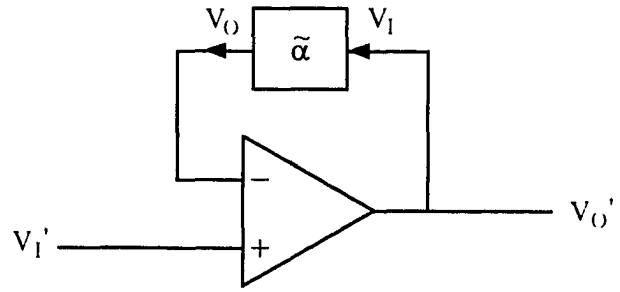


Figure 2.5: Amplifier consisting of an op-amp and Attenuator I in the feedback loop

$$V_O' = \tilde{\alpha}^{-1}(V_I') = \frac{1}{\alpha}V_I' + V_{TON} \quad . \tag{2.40}$$

The offset inherent in Attenuator I causes the amplifier to have different input and output operating points.

For the input of $V_I' = V_{IQ}' + v_I'$, the Taylor's series expansion of the output of the amplifier given from (2.5) when V_O is replaced by V_I' and V_I by V_O', is

$$V_O' = \tilde{\alpha}^{-1}(V_I') = V_{OQ}' + \left(\frac{dV_O'}{dV_I'}\right)_Q v_I' + \frac{1}{2}\left(\frac{d^2V_O'}{dV_I'^2}\right)_Q v_I'^2 + \ldots \tag{2.41}$$

where $V_{OQ}' = \tilde{\alpha}^{-1}(V_{IQ}') = V_{IQ}$,

$$\left(\frac{dV_O'}{dV_I'}\right)_Q = \frac{1}{\alpha} \quad , \tag{2.42}$$

where α is given by (2.10), and

$$\left(\frac{d^2V_O'}{dV_I'^2}\right)_Q = \frac{R(\frac{2}{\alpha}-1)-\left(\frac{1}{\alpha}-1-\frac{\gamma}{2\sqrt{\phi+V_{IQ}'}}\right)-\left\{V_{OQ}'-V_{TON}-V_{IQ}'-\gamma\left(\sqrt{\phi+V_{IQ}'}-\sqrt{\phi}\right)\right\}\frac{\gamma}{4\left(\phi+V_{IQ}'\right)^{\frac{3}{2}}}}{-RV_{IQ}'+\left\{V_{OQ}'-V_{TON}-V_{IQ}'-\gamma\left(\sqrt{\phi+V_{IQ}'}-\sqrt{\phi}\right)\right\}} \quad . \quad (2.43)$$

Note, the small signal gain of the amplifier is just the mathematical reciprocal of the attenuator's attenuation factor in the feedback loop.

If $v_I' = A'\sin\omega t$, then taking only the first three terms in (2.41), we obtain

$$V_O' \cong h_0' + h_1' \sin\omega t + h_2' \cos 2\omega t \quad , \quad (2.44)$$

where

$$h_0' = V_{OQ}' + \frac{1}{4}\left(\frac{d^2V_O'}{dV_I'^2}\right)_Q A'^2 \quad , \quad (2.45)$$

$$h_1' = \left(\frac{dV_O'}{dV_I'}\right)_Q A' = \frac{1}{\alpha}A' \quad , \quad (2.46)$$

and

$$h_2' = -\frac{1}{4}\left(\frac{d^2V_O'}{dV_I'^2}\right)_Q A'^2 \quad . \quad (2.47)$$

In these expressions, h_0' is the total dc, h_1' is the "desired" ac signal, and h_2' is the 2nd harmonic distortion component of the output of the amplifier, respectively. Again, note that the 2nd-order distortion introduces an additional dc offset as shown in (2.45), which will generally be very small. Using (2.5), (2.10), and (2.42), the small signal gain of the amplifier and the output dc operating voltage for a given R and input dc operating voltage, or the necessary R and the output dc operating voltage for a given small signal gain and

input dc operating voltage can be calculated. Then, using (2.43), (2.46), and (2.47), the desired signal output and the 2nd harmonic distortion of the output can be calculated for a given input signal amplitude.

Since the transfer function of the amplifier is the inverse function of the transfer function of the attenuator, the output noise voltage of the amplifier is the input referred noise voltage of the attenuator given by $\frac{1}{\alpha} v_{NO}$, where v_{NO} is given by (2.24)-(2.26).

2.2.6 Design and performance of Attenuator I and amplifier employing it

The design of Attenuator I for a given attenuation factor, α, is considered in this section. The dc operating point, harmonic distortion, power dissipation, output noise, area, and high frequency performance are considered in the design and performance. The performances of the designed attenuator and the amplifier employing the designed attenuator in the feedback loop are calculated and discussed in terms of the harmonic distortion and output noise.

For a given α from (2.5) and (2.10), the required value of R and the resultant V_{OQ} are calculated as a function of the input operating point, V_{IQ}. For α=0.1 in the common substrate case, the calculated results are shown in column (c) and (b) in Table 2.2. The calculations in this section again assume the parameter values in Table 2.1. The parameter values are standard for a 2μ p-well CMOS process. From (2.11), $\left(\frac{d^2V_O}{dV_I^2}\right)_Q$ is calculated and given in column (d) in Table 2.2. Note that for a given α and operating point, $\left(\frac{d^2V_O}{dV_I^2}\right)_Q$ is fixed. Likewise, $\left(\frac{d^2V_O'}{dV_I'^2}\right)_Q$ is calculated from (2.43) and shown in column

Table 2.2. Calculated results for α=0.1; (a) input operating point, (b) corresponding output operating point, (c) corresponding R, (d) $\tilde{\alpha}''$, (e) signal to 2nd harmonic distortion ratio of the output of the attenuator at A=100mV, (f) $(\tilde{\alpha}^{-1})''$, (g) signal to 2nd harmonic distortion ratio of the output of the amplifier at A'=10mV

(a)	(b)	(c)	(d)	(e)	(f)	(g)
V_{IQ} [V]	V_{OQ} [V]	R	$\left(\frac{d^2V_O}{dV_I^2}\right)_Q\left[\frac{1}{V}\right]$	$\lvert h_1/h_2\rvert$ [dB]	$\left(\frac{d^2V_O'}{dV_I'^2}\right)_Q\left[\frac{1}{V}\right]$	h_1'/h_2' [dB]
1	0.02229	3.9529	0.005019	58.0	-0.5912	76.6
1.5	0.07218	3.9649	0.004388	59.2	-0.4414	79.1
2	0.1220	3.9744	0.003970	60.1	-0.4219	79.5
2.5	0.1717	3.9847	0.003565	61.0	-0.3525	81.1
3	0.2214	3.9923	0.003264	61.8	-0.3366	81.5
3.5	0.2710	4.0005	0.002982	62.6	-0.2997	82.5
4	0.3206	4.0072	0.002750	63.3	-0.2803	83.1
4.5	0.3701	4.0144	0.002535	64.0	-0.2514	84.0
5	0.4196	4.0207	0.002351	64.6	-0.2309	84.8

(f) in Table 2.2. Remember that $V_{IQ}' = V_{OQ}$, $V_{OQ}' = V_{IQ}$. Also, $\left(\frac{d^2V_O'}{dV_I'^2}\right)_Q$ is fixed for a given gain and dc operating point. From (2.14), (2.15), (2.46), and (2.47), the signal to second harmonic distortion ratio for the attenuator and for the amplifier are given, respectively, by

$$\frac{h_1}{h_2} = -\frac{4\alpha}{\left(\frac{d^2V_O}{dV_I^2}\right)_Q A}, \tag{2.48}$$

and

$$\frac{h_1'}{h_2'} = -\frac{4\frac{1}{\alpha}}{\left(\frac{d^2V_O'}{dV_I'^2}\right)_Q A'}. \tag{2.49}$$

Note, the output signal to 2nd harmonic distortion ratio is inversely proportional to the amplitude of the input signal. The calculated signal to 2nd harmonic distortion ratios for the attenuator, when A=100mV (0-P), and for the amplifier, when A'=10mV (0-P), are shown in columns (e), and (g), respectively, in Table 2.2. The signal to 2nd harmonic distortion ratio is 61.8dB for the attenuator and 81.5dB for the amplifier at $V_{IQ} = V_{OQ}'$=3V, and these improve as the dc operating voltage increases in both the attenuator and the amplifier.

Once R=W_1L_2/L_1W_2 is fixed for a given α and dc operating point, the respective W_1, L_1, W_2, and L_2 values can be determined for minimum power dissipation, less output noise and better matching, or for minimum power dissipation, smaller area and better high frequency performance, within a given range of L and W. The average power dissipation, P_d, of the attenuator is given by $V_{DD}I_D$, where V_{DD} is assumed to be given and I_D is given

by (2.3) or (2.4). Thus, for minimum power dissipation, the ratios W_1/L_1 and W_2/L_2 should be minimized. For a given range of L and W, first W_2/L_2 is set to a minimum, W_{min}/L_{max}, since W_2/L_2 is smaller than $W_1/L_1=(W_2/L_2)\times R$ in practical cases, where R is larger than 1. For W_1 and L_1, there are two different possible choices within the given range of W and L, and for a given value of R: Choice I: $W_1=W_{min}R$ and $L_1=L_{max}$; Choice II: $W_1=W_{min}$ and $L_1=L_{max}/R$, as shown in Fig. 2.6. Choice I gives less output noise, since L_1 is larger in (2.24) and better matched performance when actually fabricated. On the other hand, Choice II gives a smaller area and better high frequency performance. For α=0.1 and several ranges of L and W, the output noise voltage, v_{NO}, and the power dissipation, P_d, of the attenuators designed as described above are calculated as a function of input dc operating voltage, V_{IQ}, using (2.24) and (2.3), and are shown in Table 2.3. In the calculations, V_{DD}=5V, T=298K, and a noise band of f_1=100Hz to f_2=1MHz along with

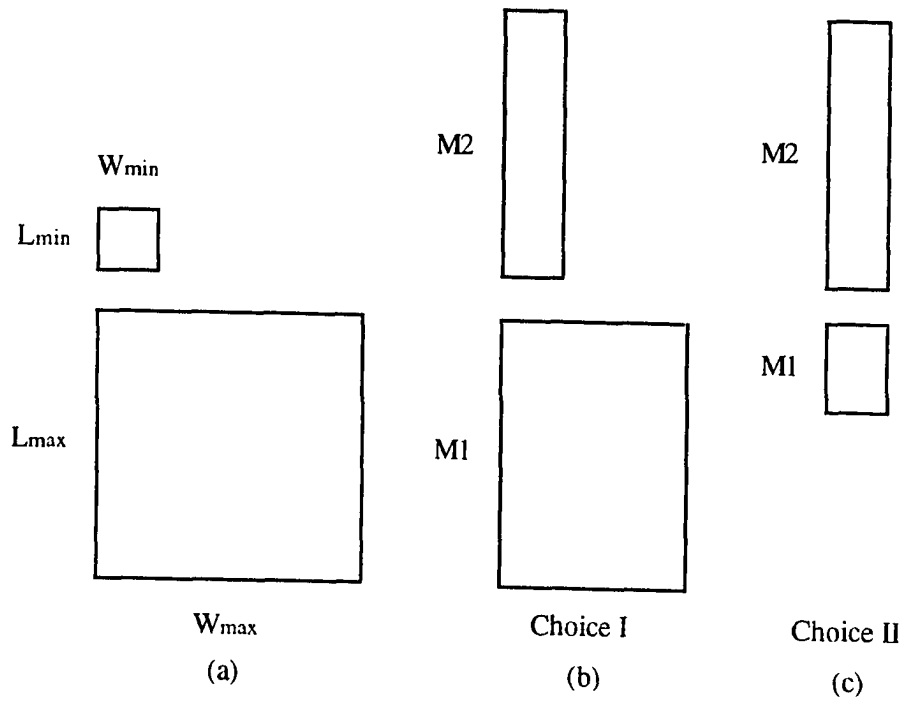


Figure 2.6: Two possible choices for the dimensions of Attenuator I

Table 2.3. Calculated results for output noise voltage, v_{NO}, and power dissipation, P_d of the designed Attenuator I; α=0.1, W_{min}=L_{min}=2μm,
Choice I : W_1=$W_{min}R$, L_1=L_{max}; W_2=W_{min}, and L_2=L_{max}.
Choice II : W_1=W_{min}, L_1=L_{max}/R; W_2=W_{min} and L_2=L_{max}.

V_{IO} [V] / L_{max} W_{max}[μm]	Choice	1		2		3		4		5	
		v_{NO} [V_{rms}]	P_d [μW]	v_{NO} [V_{rms}]	P_d [μW]	v_{NO} [V_{rms}]	P_d [μW]	v_{NO} [V_{rms}]	P_d [μW]	v_{NO} [V_{rms}]	P_d [μW]
10	I	3.64E-5	1.06	1.84E-5	31.9	1.54E-5	106	1.42E-5	223	1.34E-5	383
	II	4.66E-5		3.45E-5		3.32E-5		3.27E-5		3.26E-5	
100	I	1.10E-4	0.106	4.73E-5	3.19	3.52E-5	10.6	2.93E-5	22.3	2.57E-5	38.3
	II	1.11E-4		4.82E-5		3.64E-5		3.08E-5		2.74E-5	
1000	I	3.48E-4	0.0106	1.49E-4	0.319	1.11E-4	1.06	9.21E-5	2.23	8.06E-5	3.83
	II	3.48E-4		1.49E-4		1.11E-4		9.21E-5		8.06E-5	
10000	I	1.10E-3	0.00106	4.71E-4	0.0319	3.50E-4	0.106	2.91E-4	0.223	2.55E-4	0.383
	II	1.10E-3		4.71E-4		3.50E-4		2.91E-4		2.55E-4	

the parameter values in Table 2.1 are used. From Table 2.3, it is seen that the output noise slightly decreases, but the power dissipation increases as the operating voltage increases, and, on the other hand, the output noise increases but the power dissipation decreases as the maximum size of the transistors increases.

For a given dc operating point, the dynamic range defined by

$$\text{DR} = \frac{\text{output signal at 1\% THD}}{\text{in - band output noise}} \tag{2.50}$$

can be calculated from the results in Tables 2.2 and 2.3. If we choose $V_{IQ} = V_{OQ}{}' = 3\text{V}$ for maximum signal swing and select Choice I with a range of 2-10μm for L and W, then $\left(\frac{d^2V_O}{dV_I{}^2}\right)_Q = 0.003264\text{V}^{-1}$, $v_{NO} = 1.54\text{X}10^{-5}\text{V(rms)}$ and $P_d = 106\mu\text{W}$ for the attenuator, and $\left(\frac{d^2V_O{}'}{dV_I{}'^2}\right)_Q = -0.3366\text{V}^{-1}$ and $\frac{1}{\alpha}v_{NO} = 1.54\text{X}10^{-4}\text{V(rms)}$ for the amplifier. Thus, from (2.48) and (2.49), $\left|h_2/h_1\right| = 1\%$ at $A = 1.23\text{V}$ (0-P), and $\left|h_2'/h_1'\right| = 1\%$ at $A' = 1.189\text{V}$ (0-P). Using (2.14) and (2.50), we obtain DR=75.0dB for the attenuator. $A' = 1.189\text{V}$ (0-P) will saturate the output of the amplifier. The maximum input amplitude applicable to the amplifier is $A' \cong 0.2\,\text{V}$ (0-P) which results in 0.168% THD. From (2.46), at 0.168% THD, the dynamic range with a more stringent THD in (2.50) is DR=79.3dB.

Although the dynamic range defined as an output signal to in-band output noise ratio is widely used to characterize linear circuits, it gives little insight into the relationship between desired signal energy and total unwanted energy at the output. An alternative criteria proposed in [7] for characterizing the performance is the ratio maximum of the signal output to the total non-signal output defined by

$$\mathrm{STNR} \equiv \left| \frac{signal \quad output}{non-signal \quad output} \right|_{\max}$$

$$= \left| \frac{output \quad signal}{\sqrt{(total \quad output \quad distortion)^2 + (output \quad noise)^2}} \right|_{\max}, \tag{2.51}$$

which can be approximated to be

$$\mathrm{STNR} \cong \left| \frac{h_1}{\sqrt{h_2^{\,2} + 2v_{NO}^{\,2}}} \right|_{\max} \quad \text{or} \quad \left| \frac{h_1'}{\sqrt{h_2^{\,\prime 2} + 2v_{NO}^{\,\prime 2}}} \right|_{\max}, \tag{2.52}$$

when the second order distortion is dominant and the higher order distortion is negligible. Substituting (2.14) and (2.15) into (2.52),

$$\mathrm{STNR} \cong \left| \frac{\alpha A}{\sqrt{\left(\frac{1}{4} \left(\frac{d^2 V_O}{dV_I^2} \right)_Q A^2 \right)^2 + 2v_{NO}^2}} \right|_{\max} = \left| \frac{\alpha}{\sqrt{\frac{1}{16} \left(\frac{d^2 V_O}{dV_I^2} \right)_Q^2 A^2 + \frac{2v_{NO}^2}{A^2}}} \right|_{\max}$$

$$= \frac{|\alpha| A_{opt}}{2v_{NO}}, \tag{2.53}$$

where

$$A_{opt} = \sqrt{\frac{\sqrt{2} v_{NO}}{\frac{1}{4} \left(\frac{d^2 V_O}{dV_I^2} \right)_Q}}. \tag{2.54}$$

Since α, $\left(\frac{d^2V_O}{dV_I^2}\right)_Q$ and v_{NO} are not dependent upon A, it follows from (2.53) that the maximum ratio of the signal out to the total non-signal output occurs at the input amplitude where the magnitude of the second harmonic distortion of the output is the same as the magnitude of the output noise, if the second harmonic distortion is dominant over the higher order harmonic distortions. For the same dc operating point and conditions as used above, STNR=54.5dB at A=163mv for the attenuator, and STNR=64.4 dB at A' =50.9mV for the amplifier.

2.3 Attenuator II and Finite Gain Amplifier Employing It

Although Attenuator I investigated in the previous section has many nice characteristics, it does not have an offset adjustability. Thus it is useful only in special cases. The attenuator presented in this section has an offset adjustability independent of the attenuation ratio, in addition to the merits of Attenuator I. The circuit was originally proposed as an example of a simple amplifier [37], but when the circuit has a large gain as an amplifier, its usefulness is limited because the offset adjustability is restricted and the linearity is degraded.

The operation principle, harmonic analysis, noise analysis, frequency response analysis, and design and performance are presented. Design methods of the attenuator for minimum output noise and for minimum power consumption within a given range for the dimensions of the MOSFETs in the attenuator are discussed. The operation principle, harmonic distortion, and output noise of an amplifier using this attenuator in the feedback loop are also investigated.

2.3.1 Operation principle of Attenuator II

Two variants of the active linear inverting voltage attenuator (Attenuator II) consisting of two n-channel MOSFETs are shown in Fig. 2.7. These circuits operate as a linear inverting voltage attenuator, when both transistors are in the saturation region. Assuming the zero bias threshold voltage of both of the MOSFETs consisting the attenuator is V_{TON}, the condition will be met provided

$$V_{TON} < V_B < V_{DD} + V_{T2} \tag{2.55}$$

and

$$V_{TON} < V_I < V_O + V_{TON} \tag{2.56}$$

Under this condition, the drain currents of the transistors are given by

$$I_{D1} = K' \frac{W_1}{2L_1}(V_I - V_{TON})^2 \tag{2.57}$$

and

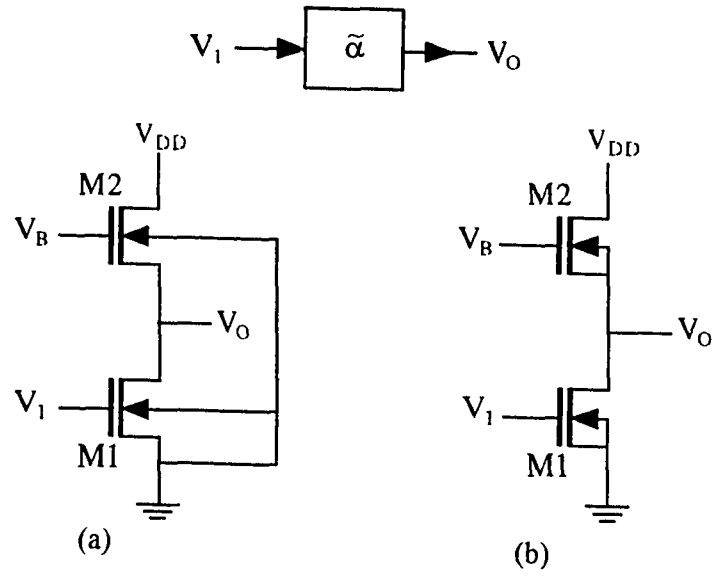


Figure 2.7: Circuit and block diagrams of Attenuator II consisting of two n-channel MOSFETs

$$I_{D2} = K' \frac{W_2}{2L_2}(V_B - V_O - V_{T2})^2, \tag{2.58}$$

where

$$V_{T2} = V_{TON} + \gamma\left(\sqrt{\phi + V_O} - \sqrt{\phi}\right). \tag{2.59}$$

Because the two drain currents should be the same for the circuit, the dc transfer function relating V_1 and V_O is obtained by equating (2.57) and (2.58).

$$V_O + \gamma\left(\sqrt{\phi + V_O} - \sqrt{\phi}\right) = -R_1 V_1 + \left\{V_B + (R_1 - 1)V_{TON}\right\}, \tag{2.60}$$

where

$$R_1 = \sqrt{\frac{W_1/L_1}{W_2/L_2}}. \tag{2.61}$$

If γ=0 in (2.60) which corresponds to the case of the circuit (b) in Fig. 2.7 where the substrate is separate, the dc transfer characteristic reduces to a linear equation,

$$V_O = \tilde{\alpha}(V_1) = \alpha V_1 + \left\{V_B - (\alpha + 1)V_{TON}\right\}. \tag{2.62}$$

In this case, the small signal attenuation factor of Attenuator II is given by

$$\alpha = -R_1, \tag{2.63}$$

which is precisely determined by the width/length ratios of the MOSFETs forming the attenuator. From (2.60) and (2.62), it is noted that the output dc operating voltage is controlled by V_B. independent of the attenuation factor in Attenuator II.

The dc transfer characteristics between V_I and V_O calculated from (2.60) for the common substrate case, R_1=0.1149 and V_B=3.993V, and the dc transfer characteristics calculated from (2.62) for the separate substrate case, R_1=0.1 and V_B=3.449V are shown in Fig. 2.8 for the range restricted by (2.56). The parameter values in Table 2.1 were used in the calculation. Note, the dc transfer function given by (2.60) for the common substrate

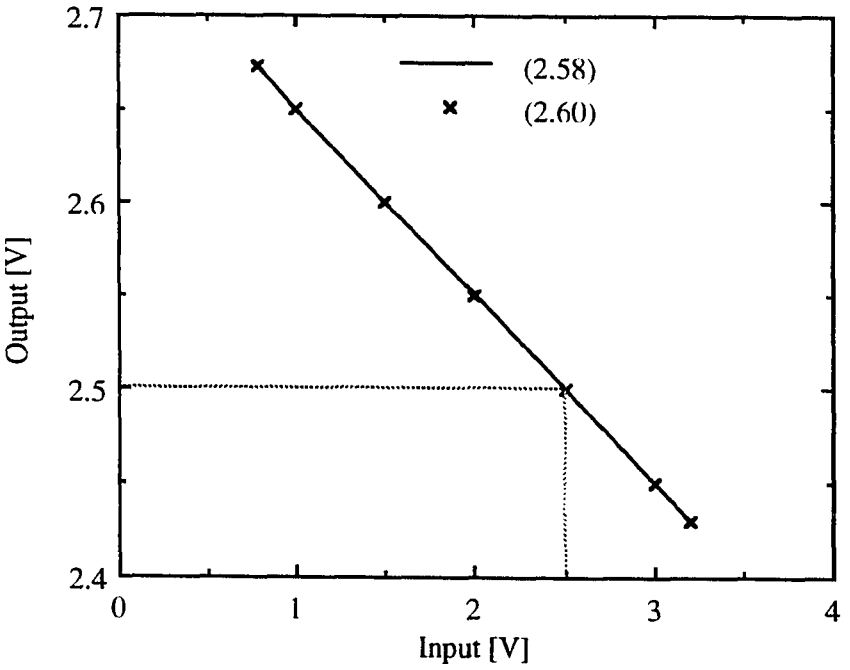


Figure 2.8: dc transfer characteristics of Attenuator II

case appears non-linear, but the degradation of linearity due to the bulk effect is not significant. The high degree of linearity shown in Fig. 2.8 suggests applications in high performance applications.

To test the dependence of the small signal attenuation factor on the process parameters, SPICE simulations using the level 1 model were performed. The small signal attenuation factor of the same common substrate attenuator, for which the dc transfer function is shown in Fig. 2.8, was simulated at an input and output dc operating voltage of 2.5V. When ϕ is increased by 10% from the value given in Table 2.1, the small signal attenuation factor increases by 0.140% and when ϕ is decreased by 10%, it decreases by 0.150%. When γ is increased by 10% from the value given in Table 2.1, the small signal attenuation factor decreases by 1.39% and when γ is decreased by 10%, it increases by 1.41%.

2.3.2 Harmonic analysis of Attenuator II

To analyze the small signal attenuation factor and the harmonic distortion of Attenuator II, the dc transfer characteristic given by (2.60) is expanded into Taylor's series about a dc operating point. For an input of $V_I = V_{IQ} + v_I$, the output, V_O, of Attenuator II is expanded as

$$V_O = \tilde{\alpha}(V_I) = V_{OQ} + \left(\frac{\partial V_O}{\partial V_I}\right)_Q v_I + \frac{1}{2}\left(\frac{\partial^2 V_O}{\partial V_I^2}\right)_Q v_I^2 + \ldots , \tag{2.64}$$

where $V_{OQ} = \tilde{\alpha}(V_{IQ})$ is given from (2.60),

$$\left(\frac{\partial V_O}{\partial V_I}\right)_Q \equiv \alpha = -R_I\left(1 + \frac{\gamma}{2\sqrt{\phi + V_{OQ}}}\right)^{-1} , \tag{2.65}$$

and

$$\left(\frac{\partial^2 V_O}{\partial V_I^2}\right)_Q = R_I^2 \frac{\gamma}{4}\left(\frac{\gamma}{2} + \sqrt{\phi + V_{OQ}}\right)^{-3} . \tag{2.66}$$

Defined by (2.65), α is the small signal attenuation factor of the attenuator for the common substrate case. Defined by (2.63) for the separate substrate case, α is a special case of γ=0 in (2.65) for the common substrate case. It is noted that the small signal attenuation factor of Attenuator II can be controlled over a wide range by the dimensions of the MOSFETs in the attenuator from (2.63) and (2.65). Once α and the dc operating point are given for a desired attenuator, the necessary R_I for a given attenuation factor is determined, using (2.65). Then, the necessary V_B to make the dc transfer characteristic curve pass through the given dc operating point is determined using (2.60).

To obtain the same dc operating voltages for the input and output, and assuming $V_{IQ} = V_{OQ} > V_{TON}(2-\alpha)/(1-\alpha)$, from (2.56) and (2.62) the maximum swing (dc operating point to peak amplitude), A_{max}, for the input is given by

$$A_{\max} = \frac{V_{TON}}{1-\alpha} \quad . \tag{2.67}$$

For $v_1 = A\sin\omega t$, from (2.64),

$$V_O \cong h_0 + h_1 \sin\omega t + h_2 \cos 2\omega t \quad , \tag{2.68}$$

where

$$h_0 = V_{OQ} + \frac{1}{4}\left(\frac{\partial^2 V_O}{\partial V_1^{\,2}}\right)_Q A^2 \quad , \tag{2.69}$$

$$h_1 = \left(\frac{\partial V_O}{\partial V_1}\right)_Q A = \alpha A \quad , \tag{2.70}$$

and

$$h_2 = -\frac{1}{4}\left(\frac{\partial^2 V_O}{\partial V_1^{\,2}}\right)_Q A^2 \quad . \tag{2.71}$$

In these expressions, h_0 is the total dc, h_1 is the "desired" ac signal, and h_2 is the 2nd harmonic distortion of the output of the attenuator. Thus, the signal to 2nd harmonic distortion ratio of the output of the attenuator is given by

$$\frac{h_1}{h_2} = -\frac{4\alpha}{\left(\frac{\partial^2 V_O}{\partial V_1^{\,2}}\right)_Q A} \quad . \tag{2.72}$$

2.3.3 Noise analysis of Attenuator II

A noise equivalent circuit of Attenuator II based on noiseless MOSFETs and output referred noise sources, and the equivalent small signal circuits are shown in Fig. 2.9. At a given dc operating point, from (2.58) and (2.59),

$$g_{m2} = \left(\frac{\partial I_{D2}}{\partial V_{GS2}}\right)_Q = K' \frac{W_2}{L_2} \left\{ V_B - V_{TON} - V_{OQ} - \left(\sqrt{\phi + V_{OQ}} - \sqrt{\phi} \right) \right\} \tag{2.73}$$

and

$$g_{mb2} = \left(\frac{\partial I_{D2}}{\partial V_{BS2}}\right)_Q = g_{m2} \frac{\gamma}{2\sqrt{\phi + V_{OQ}}} . \tag{2.74}$$

The total output conductance, g_o, is defined by

$$g_o = g_{m2} + g_{mb2} . \tag{2.75}$$

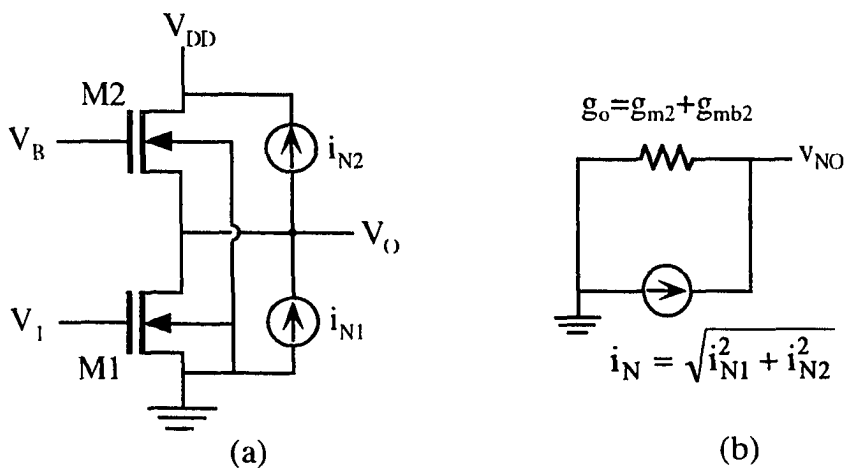


Figure 2.9: (a) Noise equivalent circuit of Attenuator II based on noiseless transistors and output noise current sources, (b) noise small signal equivalent circuit

Since both M1 and M2 are in the saturation region, the respective noise current spectral densities are given by

$$S_{I1} = S_{IT1} + S_{If1} = \frac{8}{3}kTg_{m1} + \frac{2K_f K' I_{D1Q}}{C_{OX} L_1^2 f} \quad , \tag{2.76}$$

and

$$S_{I2} = S_{IT2} + S_{If2} = \frac{8}{3}kTg_{m2} + \frac{2K_f K' I_{D2Q}}{C_{OX} L_2^2 f} \quad , \tag{2.77}$$

where, from (2.57),

$$g_{m1} = \left(\frac{\partial I_{D1}}{\partial V_{GS1}}\right)_Q = K' \frac{W_1}{L_1}\left(V_{1Q} - V_{TON}\right). \tag{2.78}$$

From Fig. 2.9 (b), the output noise voltage(rms), v_{NO}, is given by

$$v_{NO} = \frac{I_N}{g_o} = \frac{\sqrt{I_{N1}^2 + I_{N2}^2}}{g_{m2} + g_{mb2}} = \frac{\sqrt{\int_{f_1}^{f_2} S_{I1} + S_{I2} df}}{g_{m2} + g_{mb2}} \quad . \tag{2.79}$$

Substituting (2.73)-(2.78) into (2.79), we obtain

$$v_{NO} = \left[\frac{L_2}{W_2}\left\{M + N\left(\frac{1}{L_1^2} + \frac{1}{L_2^2}\right)\right\}\right]^2 \quad , \tag{2.80}$$

where M and N are functions of R_1 as defined by (2.61), operating point, noise band, and temperature given by

$$M = \frac{8kT(f_2 - f_1)\left[R_1^2\left(V_{1Q} - V_{TON}\right) + \left\{V_B - V_{TON} - V_{OQ} - \gamma\left(\sqrt{\phi + V_{OQ}} - \sqrt{\phi}\right)\right\}\right]}{3K'\left[\left\{V_B - V_{TON} - V_{OQ} - \gamma\left(\sqrt{\phi + V_{OQ}} - \sqrt{\phi}\right)\right\}\left(1 + \frac{\gamma}{2\sqrt{\phi + V_{OQ}}}\right)\right]^2} \tag{2.81}$$

and

$$N = \frac{K_f R_1^2 \left(V_{1Q} - V_{TON}\right)^2 \ln \frac{f_2}{f_1}}{C_{OX}\left[\left\{V_B - V_{TON} - V_{OQ} - \gamma\left(\sqrt{\phi + V_{OQ}} - \sqrt{\phi}\right)\right\}\left(1 + \frac{\gamma}{2\sqrt{\phi + V_{OQ}}}\right)\right]^2} \quad (2.82)$$

Thus, once R_1 required for a given attenuation factor is determined and the desired dc operating points are given, the output noise voltage(rms) for a given set of L_1, W_1, L_2, W_2, a given noise band, and temperature can be calculated using (2.80)-(2.82).

2.3.4 Frequency response analysis of Attenuator II

Figure 2.10 shows the small signal equivalent circuit of the attenuator and its reduced equivalent circuit for the case of common substrate. The parasitic capacitances involved can be modeled as

$$C_{GD1} = C_{OX} W_1 L_D \,, \quad (2.83)$$

$$C_{BD1} = \frac{C_J A_{D1}}{\left[1 + \frac{V_{OQ}}{\phi_B}\right]^{MJ}} + \frac{C_{JSW} P_{D1}}{\left[1 + \frac{V_{OQ}}{\phi_B}\right]^{MJSW}} \,, \quad (2.84)$$

$$C_{BS2} = \frac{C_J A_{S2}}{\left[1 + \frac{V_{OQ}}{\phi_B}\right]^{MJ}} + \frac{C_{JSW} P_{S2}}{\left[1 + \frac{V_{OQ}}{\phi_B}\right]^{MJSW}} + \frac{2}{3}\frac{C_J W_2 L_2}{\left[1 + \frac{V_{OQ}}{\phi}\right]^{\frac{1}{2}}} \quad (2.85)$$

and

$$C_{GS2} = C_{OX} W_2 L_D + \frac{2}{3} W_2 L_2 C_{OX} \,. \quad (2.86)$$

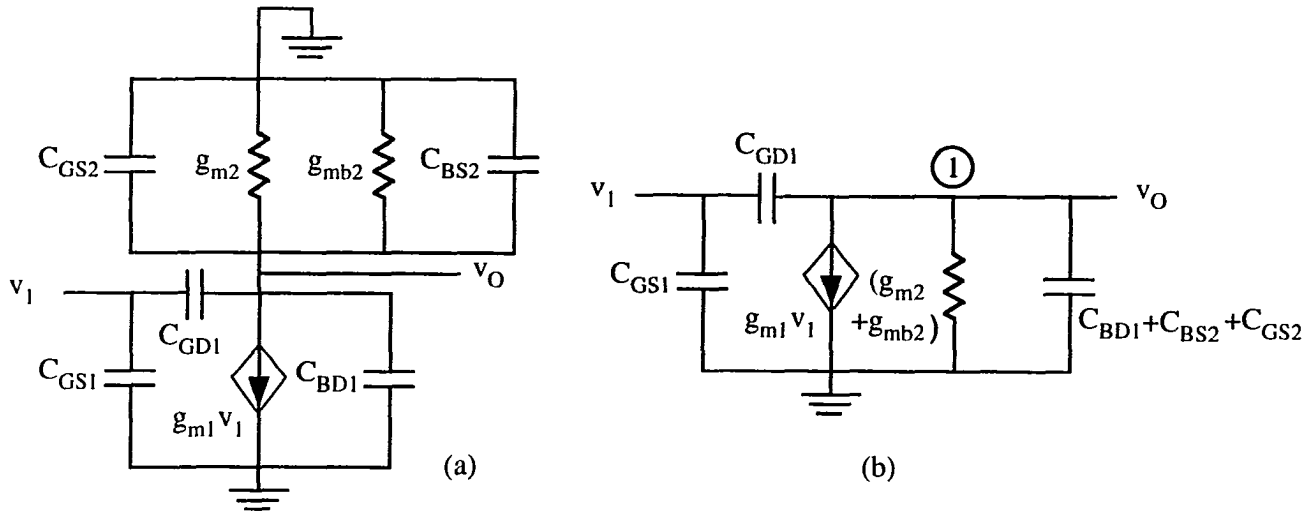


Figure 2.10: Small signal equivalent circuits of Attenuator II

Solving the node equation at node 1 in Fig. 2.10 (b), the small signal transfer function is obtained as

$$\frac{v_O(s)}{v_1(s)} \equiv F(s) = \frac{-g_{m1} + sC_{GD1}}{g_o + s(C_{GD1} + C_1)}, \tag{2.87}$$

where g_o is given by (2.75) and

$$C_1 = C_{BD1} + C_{BS2} + C_{GS2}. \tag{2.88}$$

When the substrate is separate, C_{BD2} replaces C_{BS2}. Thus, C_{BS2} in (2.88) and in Fig. 2.10 are replaced by C_{BD2}, where

$$C_{BD2} = \frac{C_J A_{D2}}{\left[1 + \frac{V_{DD} - V_{OQ}}{\phi_B}\right]^{MJ}} + \frac{C_{JSW} P_{D2}}{\left[1 + \frac{V_{DD} - V_{OQ}}{\phi_B}\right]^{MJSW}}. \tag{2.89}$$

Attenuator II, consisting of M1 23.69μmx100μm and M2 100μmx5.576μm with a common substrate, is used to calculate the 3dB bandwidth. The attenuator has a small signal attenuation factor of -0.1 and 3dB bandwidth simulated with the above model. The parameter values are listed in Table 2.1 of 93.3Mhz. In the calculation, V_{DD}=5V and V_B=3.993V were used for V_{1Q}= V_{OQ}=2.5V. The drain and source diffusion areas were assumed to be 23.69μmx4μm for M1 and 100μmx4μm for M2.

2.3.5 Analysis of finite gain amplifier employing Attenuator II

Figure 2.11 shows an amplifier employing Attenuator II in the feedback path of an op-amp. Assuming the op-amp ideal,

$$V_O' = \tilde{\alpha}^{-1}(V_I'), \tag{2.90}$$

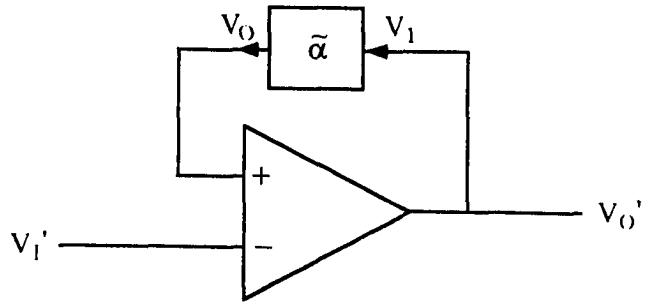


Figure 2.11: Amplifier consisting of an op-amp and Attenuator II in the feedback loop

that is, the transfer function of the amplifier is the inverse function of the transfer function of the attenuator in the feedback. Thus, the dc transfer function of the amplifier is given by (2.60), when V_1 is replaced by V_O' and V_O is replaced by V_I'. If the substrate is separate, from (2.62) V_1 replaces V_O' and V_O replaces V_I',

$$V_O' = \tilde{\alpha}^{-1}(V_I') = \frac{1}{\alpha}V_I' - \frac{1}{\alpha}\{V_B - (\alpha+1)V_{TON}\}, \tag{2.91}$$

where, in this case, the small signal attenuation factor of the attenuator in the feedback loop is α given by (2.63).

For the input of $V_I' = V_{IQ}' + v_I'$, the Taylor's series expansion of the output of the amplifier, V_O', is given by

$$V_O' = \tilde{\alpha}^{-1}(V_I') = \tilde{\alpha}^{-1}(V_{IQ}') + \left(\frac{\partial V_O'}{\partial V_I'}\right)_Q v_I' + \frac{1}{2}\left(\frac{\partial^2 V_O'}{\partial V_I'^2}\right)_Q v_I'^2 + \cdots, \tag{2.92}$$

where

$$\left(\frac{\partial V_O'}{\partial V_I'}\right)_Q = -\frac{1}{R_1}\left(1 + \frac{\gamma}{2\sqrt{\phi + V_{IQ}'}}\right) = \frac{1}{\alpha} \tag{2.93}$$

and

$$\left(\frac{\partial^2 V_O'}{\partial V_I'^2}\right)_Q = \frac{1}{R_1}\frac{\gamma}{4}(\phi + V_{IQ}')^{-\frac{3}{2}} \quad . \tag{2.94}$$

Note, the small signal gain of the amplifier given by (2.93) is the mathematical reciprocal of the attenuation factor of the attenuator in the feedback loop.

When $v_I' = A'\sin\omega t$,

$$V_O' = \left\{\tilde{\alpha}^{-1}(V_{IQ}') + \frac{1}{4}\left(\frac{\partial^2 V_O'}{\partial V_I'^2}\right)_Q A'^2\right\} + \left(\frac{\partial V_O'}{\partial V_I'}\right)_Q A'\sin\omega t - \frac{1}{4}\left(\frac{\partial^2 V_O'}{\partial V_I'^2}\right)_Q A'^2\cos 2\omega t \quad . \tag{2.95}$$

The first term in (2.95) is the total dc, the second term is the desired signal, and the third term is the second harmonic distortion of the output. Thus, the signal to the 2nd harmonic distortion ratio of the output of the amplifier is given by

$$\frac{h_1'}{h_2'} = -\frac{4\dfrac{1}{\alpha}}{\left(\dfrac{\partial^2 V_O'}{\partial V_I'^2}\right)_Q A'} \quad , \tag{2.96}$$

where h_1' is the amplitude of the fundamental frequency term and h_2' is the amplitude of the second harmonic term of the amplifier's output.

The op-amp is assumed ideal and the transfer function of the amplifier is the inverse function of the transfer function of the attenuator. Hence, the output noise voltage of the amplifier is the input referred noise voltage of the attenuator given by $\frac{1}{\alpha}v_{NO}$, where v_{NO} is given by (2.80)-(2.82).

2.3.6 Design and performance of Attenuator II and amplifier employing it

Based on the analyses in the previous sections, the design, and performance of Attenuator II for a given attenuation factor, α, a dc operating point, and the amplifier employing the attenuator in the feedback loop are discussed in this section. All calculations in this section assume the case where α=-0.1, $V_{IQ}=V_{OQ}=V_Q$ =2.5V and V_{DD}=5V and a common substrate.

For a given α, R_1 is calculated first by using (2.65) for Attenuator II. Thus, for α=-0.1, R_1=0.1149. The parameter values given in Table 2.1 are standard for a 2μm p-well CMOS process and were used in the calculations in this section. Then, using (2.60), the required V_B for a given dc operating point is calculated. V_B=3.993V for V_Q=2.5V. Now, we can determine the harmonic distortion of the attenuator by calculating $\left(\frac{\partial^2 V_O}{\partial V_I^2}\right)_Q$ given by (2.66). At the above conditions, $\left(\frac{\partial^2 V_O}{\partial V_I^2}\right)_Q$ =2.094X10^{-4}V^{-1} and the signal to 2nd harmonic distortion ratio of the output of the attenuator given by (2.72) is 85.6dB for a 100 mV (0-P) input amplitude.

Using (2.61) R_1 is determined for a given α and the respective W_1, L_1, W_2, and L_2 can be designed for minimum output noise or for minimum power dissipation under the condition of (2.61), within a given range of L and W. The output noise is related to L_1, W_2, and L_2 by (2.80), where M and N can be calculated using (2.81) and (2.82), when R_1, V_Q, a noise frequency band, and temperature are given. Using (2.80) for minimum output noise, we set $L_1=W_2=L_{max}$ and $L_2=L_{2,opt}$. The optimal $L_{2,opt}$ is given by

$$L_{2,opt} = \sqrt{\frac{N}{M+\frac{1}{L_1^2}N}} \quad . \tag{2.97}$$

Now, the remaining W_1 can be calculated such that (2.61) is satisfied.

The average power dissipation of the attenuator, P_d, is given by $P_d=I_{D1}XV_{DD}$, where I_{D1} is given by (2.57). If we now want to minimize the power dissipation from (2.57), we need to minimize W_1/L_1. Thus, we set $W_1=W_{min}$ and $L_1=L_{max}$ for minimum power dissipation. The remaining W_2 and L_2 should be chosen such that (2.61) is satisfied.

The designed dimensions of the MOSFETs, and output noise and power dissipation of the attenuator, when it is optimized for minimum output noise and for minimum power dissipation as described above for a set of L_{max} (or W_{max}), are shown in Table 2.4. For the calculation of minimum power, W_{min} was set as 2 μm. An example of the design for minimum output noise, is considered for the case where the maximum is 100 μm for L and W. First, set $L_1=W_2=100\mu m$, and then calculate L_2 using (2.97). For a noise band of $f_1=100Hz$ to $f_2=1MHz$ and $T=298K$, from (2.81) and (2.82), $M=8.2560X10^{-10}V^2$ and $N=2.5752X10^{-20}V^2m^2$. Then, from (2.97), L_2 is determined to be 5.576 μm. The remaining W_1 is calculated to match the required R_1 value and, in this case, $W_1=23.69$ μm. From (2.80) and $P_d=I_{D1}XV_{DD}$ where I_{D1} is given by (2.57), the attenuator with the transistors of these dimensions has an output noise, v_{NO}, of $9.61\mu V_{rms}$, and power dissipation, P_d, of $99.6\mu W$.

For α=-0.1 and V_{TON}=0.777V, the maximum applicable input amplitude, A_{max}, given by (2.67) is approximately 0.7V. At this maximum input and output noise voltage of $9.61\mu V_{rms}$, the signal to noise ratio is 74.2dB and the signal to THD ratio is 68.7dB (0.037%) for the attenuator. STNR of the attenuator is 68.6dB at 0.503V (0-P) input amplitude.

Table 2.4: Designed dimensions of Attenuator II, output noise and power dissipation;
(a) optimized for minimum noise, (b) optimized for minimum power

L_{max} [μm]	(a) Optimized for minimum v_{NO}				(b) Optimized for minimum P_d			
	W_1[μm] L_1[μm]	W_2[μm] L_2 [μm]	v_{NO} [μV_{rms}]	P_d[μW]	W_1[μm] L_1[μm]	W_2[μm] L_2 [μm]	v_{NO} [μV_{rms}]	P_d[μW]
10	0.2709 10	10 4.876	32.5	11.4	2 10	10 0.6604	63.0	84.1
100	23.69 100	100 5.576	9.61	99.6	2 100	100 66.04	23.5	8.41
1000	2365 1000	1000 5.585	3.04	994	2 1000	151.4 1000	73.8	0.841
10000	226500 10000	10000 5.585	0.960	9940	2 10000	151.4 10000	234	0.0841

The amplifier employing the above attenuator in the feedback loop has a gain of 10. For the amplifier, $\left(\frac{\partial^2 V_O'}{\partial V_I'^2}\right)_Q$ =0.2094V^{-1} from (2.94) and the signal to 2nd harmonic distortion ratio of the output is 85.6dB, for 10mV (0-P) input amplitude from (2.96). The output noise voltage of the amplifier is $\frac{1}{\alpha} v_{NO}$. The maximum applicable input amplitude to the amplifier is approximately 70mV (0-P). At this input amplitude, the signal to noise ratio is 74.2dB and the signal to 2nd harmonic distortion ratio is 68.7dB (0.037%) for the amplifier. STNR of the amplifier is 68.6dB at 50.3mV (0-P) input amplitude.

2.4 Summing Attenuator

The investigation in section 2.3 for Attenuator II showed the attenuator is useful in realization of a finite gain amplifier in integrated circuits. It is as easy as in discrete circuits to overcome the offset problem inherent in Attenuator I. Even though the realization of a single input finite gain amplifier becomes convenient when using Attenuator I, a summing attenuator is necessary to realize versatile multiple input finite gain amplifiers in integrated circuits as easily as in discrete circuits. In this section, a summing attenuator suitable for this purpose is discussed. Attenuator II, which demonstrated useful characteristics as a single input attenuator, can be cascaded to form multiple input attenuators. By utilizing Attenuator I and the summing attenuator discussed in this section, it is possible to construct versatile multiple input summing/subtracting amplifiers in integrated circuits.

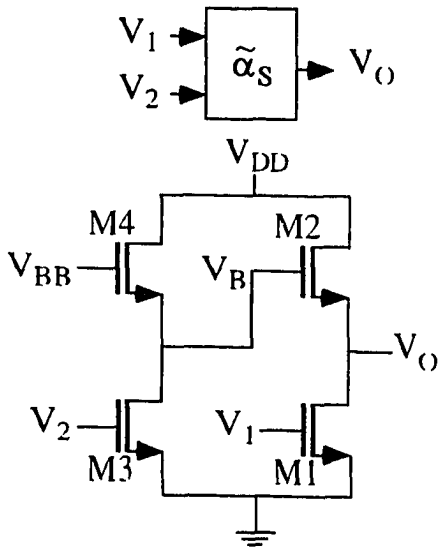


Figure 2.12: Circuit and block diagrams of summing attenuator

2.4.1 Operation principle of summing attenuator

Figure 2.12 shows a two-input active linear inverting voltage summing attenuator which consists of two single cascaded input attenuator. For the summing attenuator, V_{BB} is used to control the output dc operating voltage and input signals are designated as V_1 and V_2. It is possible to cascade more attenuators to make multiple (more than two) input summing attenuators. The fact the dc transfer function from V_B to V_O is also linear causes the cascaded attenuators to form a linear summing attenuator. It is noted that both V_B and V_1 are used as inputs to the attenuator consisting of M1 and M2.

As Attenuator II, the summing attenuator works when all the MOSFETs M1 through M4 are operating in the saturation region. Thus, the dc transfer characteristic can be obtained by equating the drain currents in the saturation region for each attenuator.

Assuming the zero bias threshold voltages of the four MOSFETs are matched at V_{TON}, the four transistors are in the saturation region provided

$$2V_{TON} + \gamma\left(\sqrt{\phi + V_{TON}} - \sqrt{\phi}\right) < V_{BB} < V_{DD} + V_{T4}, \tag{2.98}$$

$$V_{TON} < V_2 < V_B + V_{TON}, \tag{2.99}$$

and the inequality (2.56) is met. By equating the drain currents of M3 and M4 given by

$$I_{D3} = K' \frac{W_3}{2L_3}\left(V_2 - V_{TON}\right)^2 \tag{2.100}$$

and

$$I_{D4} = K' \frac{W_4}{2L_4}\left(V_{BB} - V_B - V_{T4}\right)^2, \tag{2.101}$$

where

$$V_{T4} = V_{TON} + \gamma\left(\sqrt{\phi + V_B} - \sqrt{\phi}\right), \tag{2.102}$$

the dc transfer function between V_2 and V_B is obtained as

$$V_B + \gamma\left(\sqrt{\phi + V_B} - \sqrt{\phi}\right) = -R_2 V_2 + \left\{V_{BB} + (R_2 - 1)V_{TON}\right\}, \tag{2.103}$$

where

$$R_2 = \sqrt{\frac{W_3 / L_3}{W_4 / L_4}}. \tag{2.104}$$

Similarly, the dc transfer function between V_1 and V_O is given by (2.60). Combining (2.60) and (2.103), gives the dc transfer characteristic of the summing attenuator, $\tilde{\alpha}_S$.

For the separate substrate case,

$$V_B = \tilde{\alpha}_2\left(V_2\right) = \alpha_2 V_2 + \left\{V_{BB} - (\alpha_2 + 1)V_{TON}\right\}. \tag{2.105}$$

where the small signal attenuation factor for the input V_2 is

$$\alpha_2 = -R_2 . \tag{2.106}$$

Equation (2.105) for the separate substrate case is a special case of γ=0 in (2.103) for the common substrate case. Similarly, for the separate substrate case, the dc transfer function between V_1 and V_O of the summing attenuator is given by (2.62), with α replaced by α_1 to denote the small signal attenuation factor for V_1 of the summing attenuator and $\tilde{\alpha}$ replaced by $\tilde{\alpha}_1$ to denote the dc transfer function between V_1 and V_O of the summing attenuator where

$$\alpha_1 = -R_1 . \tag{2.107}$$

In the separate case, the attenuation factors are α=-R_1 for Attenuator II, and α_1=-R_1 and α_2=-R_2 for the summing attenuator.

Combining (2.62) with α replaced by α_1 and (2.105), the dc transfer function of the summing attenuator is given by

$$V_O \equiv \tilde{\alpha}_S(V_1, V_2) = \alpha_1 V_1 + \alpha_2 V_2 + \left\{V_{BB} - (\alpha_1 + \alpha_2 + 2)V_{TON}\right\} \tag{2.108}$$

for the separate substrate case.

Even when the substrates are common, the transfer characteristics between V_1 and V_O and between V_2 and V_O are nearly linear as shown in Fig. 2.13. This fact makes the circuit shown in Fig. 2.12 useful as a voltage summing attenuator. In calculating the dc transfer characteristic, the parameter values in Table 2.1, standard for a 2μ CMOS process, were used. R_1=0.1149 and R_2=0.1290 were used so that the small signal attenuation factors for V_1 and V_2 are both -0.1. V_{BB}=5.712V was set such that, both input dc operating voltages are 2.5V. Therefore, V_{BQ}=3.993V and the output dc operating voltage become 2.5V. Figure 2.13 demonstrates the linear range when the input and

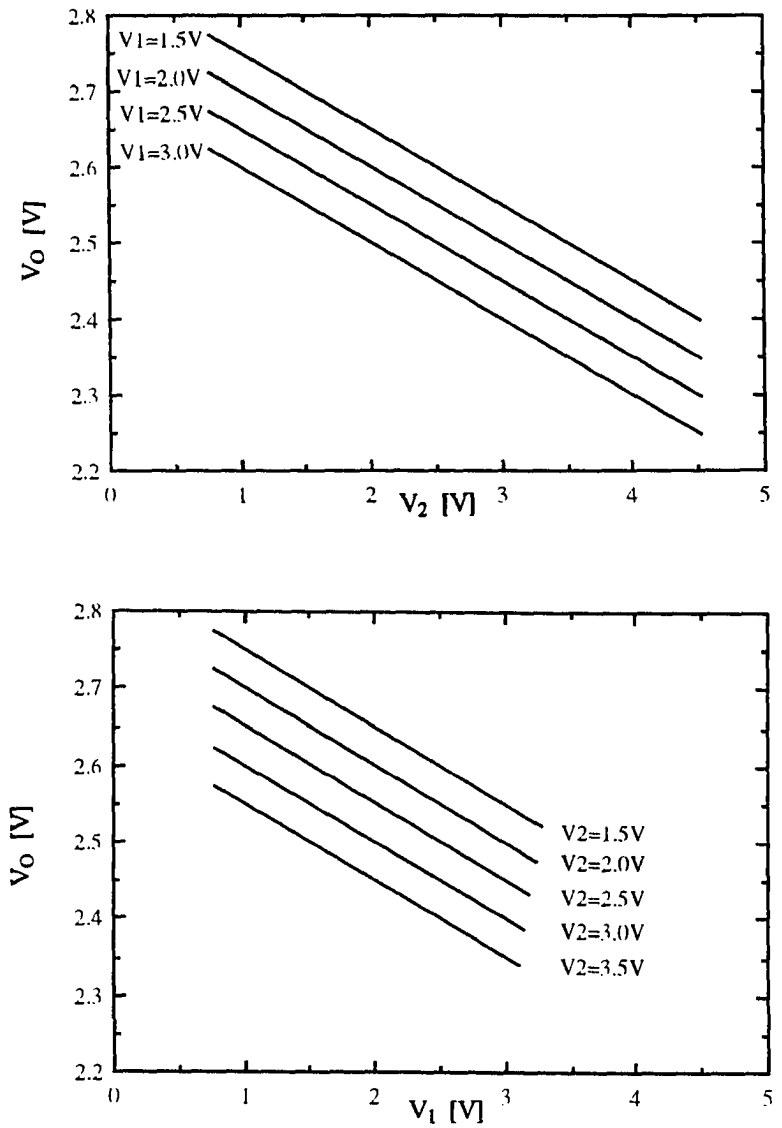


Figure 2.13: dc transfer characteristics of summing attenuator

output operating voltages are 2.5V and each small signal attenuation factor for each input is -0.1. Figure 2.13 shows also the high degree of linearity of the transfer function.

2.4.2 Harmonic and intermodulation analysis of summing attenuator

To analyze the small signal attenuation factors, and the harmonic and intermodulation distortions of the summing attenuator, the dc transfer function given by (2.60) between V_1 and V_O is expanded into a two-dimensional Taylor's series. Therefore, $V_1 = V_{1Q} + v_1$ and $V_B = V_{BQ} + v_B$, the output voltage, V_O, is expanded as

$$V_O = \tilde{\alpha}_1(V_1, V_B)$$

$$= \tilde{\alpha}_1(V_{1Q}, V_{BQ}) + \left(\frac{\partial V_O}{\partial V_1}\right)_Q v_1 + \left(\frac{\partial V_O}{\partial V_B}\right)_Q v_B + \frac{1}{2}\left(\frac{\partial^2 V_O}{\partial V_1^2}\right)_Q v_1^2 + \frac{1}{2}\left(\frac{\partial^2 V_O}{\partial V_B^2}\right)_Q v_B^2 + \left(\frac{\partial^2 V_O}{\partial V_1 \partial V_B}\right)_Q v_1 v_B + \ldots . \tag{2.109}$$

where $V_{OQ} = \tilde{\alpha}_1(V_{1Q}, V_{BQ})$ is given from (2.60), and

$$\left(\frac{\partial V_O}{\partial V_B}\right)_Q = \left(1 + \frac{\gamma}{2\sqrt{\phi + V_{OQ}}}\right)^{-1}, \tag{2.110}$$

$$\left(\frac{\partial^2 V_O}{\partial V_B^{\,2}}\right)_Q = \frac{\gamma}{4}\left(\frac{\gamma}{2} + \sqrt{\phi + V_{OQ}}\right)^{-3}, \tag{2.111}$$

and

$$\left(\frac{\partial^2 V_O}{\partial V_1 \partial V_B}\right)_Q = -R_1 \frac{\gamma}{4}\left(\frac{\gamma}{2} + \sqrt{\phi + V_{OQ}}\right)^{-3} \tag{2.112}$$

Note, the small signal attenuation factor between the input V_1 and the output given by (2.65) is controllable by adjusting R_1, while the small signal attenuation factor between V_B

and the output given by (2.110) depends only on process parameters. The small signal attenuation factor for V_B is 1 for the separate substrate case. Even if the attenuation factor between V_B and the output is uncontrollable, it is a fact that the transfer characteristic for V_B is also very linear. This makes it possible to have a summing attenuator by cascading attenuators as shown in Fig. 2.12. Thus, the circuit shown in Fig. 2.12 is an inverting voltage summing attenuator, when V_{BB} is used to control the output dc operating voltage and when V_1 and V_2 are used as inputs.

On the other hand, if $V_2=V_{2Q}+B\sin\omega_2 t$, similarly to (2.68)-(2.71)

$$V_B = V_{BQ} + v_B = \left(\tilde{\alpha}_2(V_{2Q}) + \frac{1}{4}\left(\frac{\partial^2 V_B}{\partial V_2^{\,2}}\right)_Q B^2 \right) + \left(\left(\frac{\partial V_B}{\partial V_2}\right)_Q B\sin\omega_2 t - \frac{1}{4}\left(\frac{\partial^2 V_B}{\partial V_2^{\,2}}\right)_Q B^2 \cos 2\omega_2 t \right) + \cdots \tag{2.113}$$

where $V_B = \tilde{\alpha}_2(V_2)$ is the dc transfer function of the attenuator consisting of M3 and M4 given by (2.103). In (2.113),

$$\left(\frac{\partial V_B}{\partial V_2}\right)_Q = -R_2\left(1+\frac{\gamma}{2\sqrt{\phi+V_{BQ}}}\right)^{-1} \tag{2.114}$$

and

$$\left(\frac{\partial^2 V_B}{\partial V_2^{\,2}}\right)_Q = R_2^{\,2}\,\frac{\gamma}{4}\left(\frac{\gamma}{2}+\sqrt{\phi+V_{BQ}}\right)^{-3} . \tag{2.115}$$

Substituting (2.113) into (2.109), the output of the summing attenuator, V_O, is given by

$$V_O = \tilde{\alpha}_S(V_1,V_2) = \left\{ \tilde{\alpha}_1(V_{1Q},V_{BQ}) + \frac{1}{4}\left(\frac{\partial^2 V_O}{\partial V_1^{\,2}}\right)_Q A^2 + \frac{1}{4}\left(\frac{\partial^2 V_O}{\partial V_B^{\,2}}\right)_Q \left(\frac{\partial V_B}{\partial V_2}\right)_Q^2 B^2 + \cdots \right\}$$

$$+\left\{\left(\frac{\partial V_O}{\partial V_1}\right)_Q A\sin\omega_1 t+\left(\frac{\partial V_O}{\partial V_B}\right)_Q\left(\frac{\partial V_B}{\partial V_2}\right)_Q B\sin\omega_2 t\right\}$$

$$-\left\{\frac{1}{4}\left(\frac{\partial^2 V_O}{\partial V_1^2}\right)_Q A^2\cos 2\omega_1 t+\frac{1}{4}\left(\left(\frac{\partial V_O}{\partial V_B}\right)_Q\left(\frac{\partial^2 V_B}{\partial V_2^2}\right)_Q+\left(\frac{\partial^2 V_O}{\partial V_B^2}\right)_Q\left(\frac{\partial V_B}{\partial V_2}\right)_Q^2\right)B^2\cos 2\omega_2 t+\ldots\right\}$$

$$+\left\{\frac{1}{2}\left(\frac{\partial^2 V_O}{\partial V_1\partial V_B}\right)_Q\left(\frac{\partial V_B}{\partial V_2}\right)_Q AB\cos(\omega_1-\omega_2)t-\frac{1}{2}\left(\frac{\partial^2 V_O}{\partial V_1\partial V_B}\right)_Q\left(\frac{\partial V_B}{\partial V_2}\right)_Q AB\cos(\omega_1+\omega_2)t+\ldots\right\}. \tag{2.116}$$

The first term in (2.116) is the total dc, the second term is the "desired" signal, the third term is the harmonic distortion, and the fourth term is the intermodulation distortion of the output of the summing attenuator. From (2.116), it is seen that the second harmonic distortion also introduces an additional dc offset which will be generally very small. From the second term in (2.116), the small signal attenuation factor for V_1, α_1, is given by (2.65) and the small signal attenuation factor for V_2 is given by

$$\alpha_2=\left(\frac{\partial V_O}{\partial V_B}\right)_Q\left(\frac{\partial V_B}{\partial V_2}\right)_Q=R_2\left(1+\frac{\gamma}{2\sqrt{\phi+V_{OQ}}}\right)^{-1}\left(1+\frac{\gamma}{2\sqrt{\phi+V_{BQ}}}\right)^{-1}. \tag{2.117}$$

Using the same summing attenuator the dc transfer characteristic was calculated and plotted in Fig. 2.13, the signal to 2nd harmonic distortion ratio is calculated as 77.9dB, when both the input signal amplitudes are 100mV (0-P) and when the frequency of both inputs are the same.

2.4.3 Noise analysis of summing attenuator

Figure 2.14 shows a noise equivalent circuit of the summing attenuator based on noiseless transistors, output referred noise sources, and a simplified equivalent circuit. Similar to (2.79), the output noise voltage (rms) , v_{NO}' , of the attenuator consisting of M3 and M4 is given by

$$v_{NO}' = \frac{\sqrt{I_{N3}^2 + I_{N4}^2}}{g_{m4} + g_{mb4}} = \frac{\sqrt{\int_{f_1}^{f_2} S_{I3} + S_{I4} df}}{g_{m4} + g_{mb4}} \quad , \tag{2.118}$$

where

$$g_{m4} = \left(\frac{\partial I_{D4}}{\partial V_{GS4}}\right)_Q = K' \frac{W_4}{L_4} \left\{ V_{BB} - V_{TON} - V_{BQ} - \gamma \left(\sqrt{\phi + V_{BQ}} - \sqrt{\phi} \right) \right\} \quad , \tag{2.119}$$

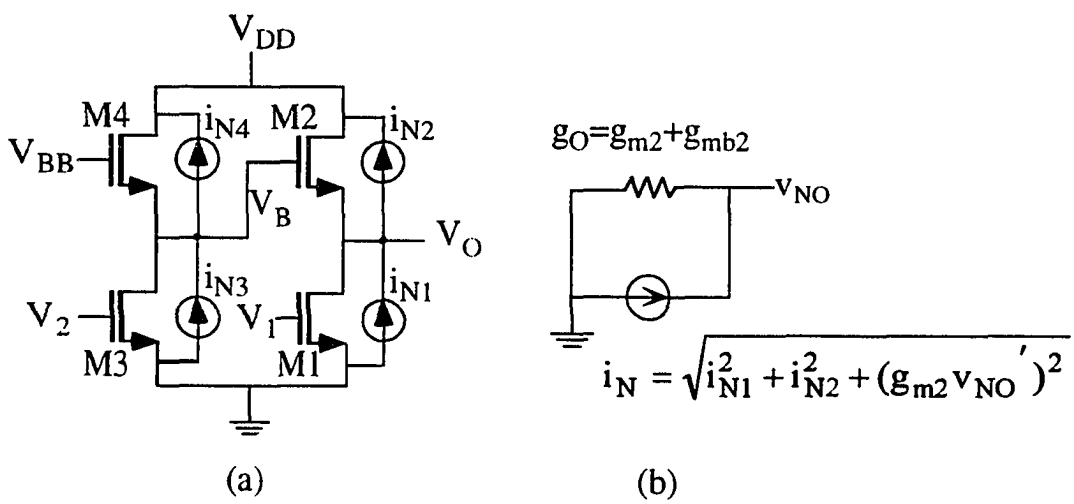


Figure 2.14: (a) Noise equivalent circuit of summing attenuator based on noiseless transistors and output noise current sources, (b) noise small signal equivalent circuit

$$g_{mb4} = \left(\frac{\partial I_{D4}}{\partial V_{BS4}}\right)_Q = g_{m4}\frac{\gamma}{2\sqrt{\phi + V_{BQ}}} \quad , \tag{2.120}$$

$$S_{I3} = \frac{8}{3}kTg_{m3} + \frac{2K_f K' I_{D3Q}}{C_{OX} L_3^2 f} \quad , \tag{2.121}$$

$$S_{I4} = \frac{8}{3}kTg_{m4} + \frac{2K_f K' I_{D4Q}}{C_{OX} L_4^2 f} \quad , \tag{2.122}$$

and

$$g_{m3} = \left(\frac{\partial I_{D3}}{\partial V_{GS3}}\right)_Q = K'\frac{W_3}{L_3}\left(V_{2Q} - V_{TON}\right) \quad . \tag{2.123}$$

Then, from Fig. 2.14, the output noise voltage (rms), v_{NO}, of the summing attenuator is given by

$$v_{NO} = \frac{I_N}{g_O} = \frac{\sqrt{I_{N1}^2 + I_{N2}^2 + (g_{m2}V_{NO}')^2}}{g_O} = \frac{\sqrt{I_{N1}^2 + I_{N2}^2 + \left(\frac{g_{m2}}{g_{m4}+g_{mb4}}\right)^2\left(I_{N3}^2 + I_{N4}^2\right)}}{g_{m2}+g_{mb2}}$$

$$= \frac{\sqrt{\int_{f_1}^{f_2} S_{I1} + S_{I2}df + \left(\frac{g_{m2}}{g_{m4}+g_{mb4}}\right)^2 \int_{f_1}^{f_2} S_{I3} + S_{I4}df}}{g_{m2}+g_{mb2}} \tag{2.124}$$

For given attenuation factors, R_1 and R_2 are determined. Then, the dimensions (W and L) of each MOSFET in the summing attenuator can be optimized for minimum output noise or for minimum power dissipation using the same scheme as discussed in section 2.3.6 under the restrictions of (2.61) and (2.104). Consider α_1=α_2=-0.1 and the separate substrate case for the calculation of the output noise when it is minimized with the design scheme in section 2.3.6. R_1=R_2=0.1 and V_{BB}=4.398V (V_{BQ}=3.449V) for the same input

and output operating voltages. The parameter values in Table 2.1 are used. When the allowable maximum for L and W of the MOSFETs is 100μm, the optimized sizes for minimum noise are W_1=W_3=15.59μm, L_1=L_3=W_2=W_4=100μm, and L_2=L_4=6.415μm. The summing attenuator consisting of these transistors has an output noise, v_{NO}, of 1.7864X10^{-5}V(rms) and power dissipation, P_d, of 131μW. Thus, when both input amplitudes are 0.7V (0-P), the maximum for v_1, DR=74.9dB.

2.4.4 Frequency response analysis of summing attenuator

Figure 2.15 shows the reduced small signal equivalent circuit of the summing attenuator for the case of a common substrate. Parasitic capacitances, other than the capacitances defined before, can be modeled as

$$C_{GD3} = C_{OX} W_3 L_D \ , \tag{2.125}$$

$$C_{BD3} = \frac{C_J A_{D3}}{\left[1 + \frac{V_{BQ}}{\phi_B}\right]^{MJ}} + \frac{C_{JSW} P_{D3}}{\left[1 + \frac{V_{BQ}}{\phi_B}\right]^{MJSW}} \ , \tag{2.126}$$

$$C_{GS4} = C_{OX} W_4 L_D + \frac{2}{3} W_4 L_4 C_{OX} \ , \tag{2.127}$$

$$C_{BS4} = \frac{C_J A_{S4}}{\left[1 + \frac{V_{BQ}}{\phi_B}\right]^{MJ}} + \frac{C_{JSW} P_{S4}}{\left[1 + \frac{V_{BQ}}{\phi_B}\right]^{MJSW}} + \frac{2}{3} \frac{C_J W_4 L_4}{\left[1 + \frac{V_{BQ}}{\phi}\right]^{2}} \ , \tag{2.128}$$

and

$$C_{GD2} = C_{OX} W_2 L_D \ . \tag{2.129}$$

Solving the node equations at nodes 1 and 2 in Fig. 2.15, the small signal transfer function of the summing attenuator is obtained as

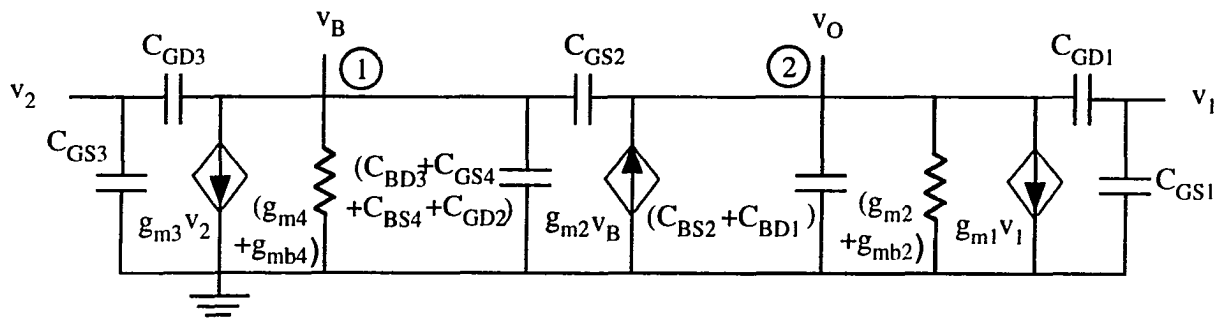


Figure 2.15: Small signal equivalent circuit of summing attenuator

$$v_O(s) = -\frac{(g_{m1} - sC_{GD1})(g_2 + sC_2)v_1(s) + (g_{m3} - sC_{GD3})(g_1 + sC_{GS2})v_2(s)}{g_1 g_2 + s(g_1 C_3 + g_2 C_4) + s^2\left(C_2 C_4 - C_{GS2}{}^2\right)}, \quad (2.130)$$

where

$$g_2 = g_{m4} + g_{mb4}, \quad (2.131)$$

$$C_2 = C_{GS4} + C_{BS4} + C_{GD3} + C_{BD3} + C_{GS2} + C_{GD2}, \quad (2.132)$$

$$C_3 = C_{GS4} + C_{BS4} + C_{GD3} + C_{BD3} + C_{GD2} \quad (2.133)$$

and

$$C_4 = C_{GS2} + C_{BS2} + C_{GD1} + C_{BD1}. \quad (2.134)$$

When the substrate is separate, C_{BD2} replaces C_{BS2}, and C_{BD4} replaces C_{BS4}. Thus, C_{BS2} and C_{BS4} in (2.132)-(2.134) and in Fig. 2.15 should be replaced by C_{BD2} and C_{BD4}, respectively, where

$$C_{BD4} = \frac{C_J A_{D4}}{\left[1 + \frac{V_{DD} - V_{BQ}}{\phi_B}\right]^{MJ}} + \frac{C_{JSW} P_{D4}}{\left[1 + \frac{V_{DD} - V_{BQ}}{\phi_B}\right]^{MJSW}}. \quad (2.135)$$

A summing attenuator consisting of M1 15.59μmx100μm, M2 100μmx6.415μm, M3 15.59μmx100μm, and M4 100μmx6.415μm with separate substrates is used for the calculation of the 3dB bandwidth. The summing attenuator has a small signal attenuation factor of -0.1 for both inputs. The 3dB bandwidth simulated with the above model and the parameter values in Table 2.1 is 93.5Mhz, when a signal is applied to both inputs. In the calculation, V_{DD}=5V and V_{BB}=4.398V for V_{1Q}=V_{2Q}=V_{OQ}=2.5V were used. The drain

and source diffusion areas were assumed to be 15.59μmx4μm for M1 and M3, and 100μmx4μm for M2 and M4.

2.5 Summing and Subtracting Amplifiers

The summing and subtracting amplifier structures using the inverting attenuator and the inverting summing attenuator along with an op-amp are shown in Fig. 2.16. In Fig. 2.16, the circuit (a) functions as summing amplifiers and the circuit (b) functions as a subtracting amplifier. To derive the function of each circuit in Fig. 2.16, assume an ideal op-amp and a separate substrate case. If the substrate is common, the functions are more complicated. They use the bulk effect terms.

For the circuit (a) in Fig. 2.16, the inputs to the op-amp are expressed as

$$V_- = \alpha_1 V_1 \alpha_2 V_2 + \{V_{BB} - (\alpha_1 + \alpha_2 + 2)V_{TON}\} \tag{2.136}$$

and

$$V_+ = \alpha V_{OA} + \{V_B - (\alpha + 1)V_{TON}\} \quad . \tag{2.137}$$

By equating V_- and V_+, the outputs are given by

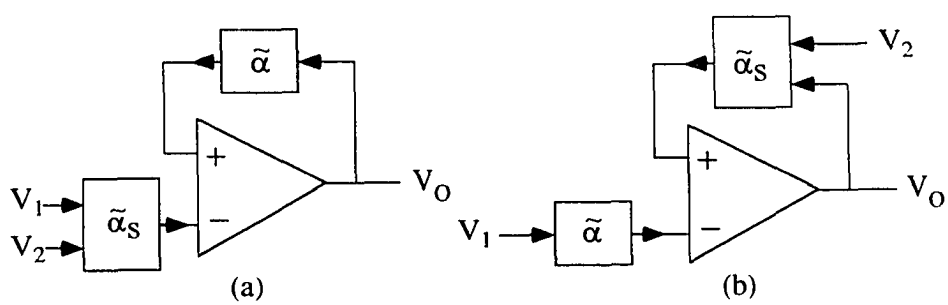


Figure 2.16: (a) Summing amplifier, (b) subtracting amplifier

$$V_{OA} = \frac{\alpha_1}{\alpha} V_1 + \frac{\alpha_2}{\alpha} V_2 + \frac{1}{\alpha}\left\{V_{BB} - V_B - (\alpha_1 + \alpha_2 - \alpha + 1)V_{TON}\right\} \qquad (2.138)$$

From (2.138), the circuit in Fig. 2.16 (a) is a summing amplifier with a wide range of available gain for each input.

Similarly, for the circuit (b) in Fig. 2.16, the output is given by

$$V_{OB} = \frac{\alpha}{\alpha_2} V_1 - \frac{\alpha_1}{\alpha_2} V_2 - \frac{1}{\alpha_2}\left\{V_{BB} - V_B - (\alpha_1 + \alpha_2 - \alpha + 1)V_{TON}\right\} \qquad (2.139)$$

From (2.139), the circuit in Fig. 2.16 (a) is a subtracting amplifier with a wide range of available gain for each input.

2.6 Multiple Input Summing and Subtracting Amplifiers

It is possible to construct multiple (more than two) input summing and subtracting amplifiers. A three-input and a four-input summing amplifier using the two-input summing amplifier, shown in Fig. 2.16 (a) as a basic building block, are shown in Fig. 2.17. For the three-input summing amplifier shown in Fig. 2.17 (a),

$$v_O = \frac{\alpha_{11}\alpha_{21}}{\alpha_{f1}\alpha_{f2}} v_1 + \frac{\alpha_{12}\alpha_{21}}{\alpha_{f1}\alpha_{f2}} v_2 + \frac{\alpha_{22}}{\alpha_{f2}} v_3 \,. \qquad (2.140)$$

For the four-input summing amplifier shown in Fig. 2.17 (b),

$$v_O = \frac{\alpha_{11}\alpha_{31}}{\alpha_{f1}\alpha_{f3}} v_1 + \frac{\alpha_{12}\alpha_{31}}{\alpha_{f1}\alpha_{f3}} v_2 + \frac{\alpha_{21}\alpha_{32}}{\alpha_{f2}\alpha_{f3}} v_3 + \frac{\alpha_{22}\alpha_{32}}{\alpha_{f2}\alpha_{f3}} v_4 \,. \qquad (2.141)$$

If the multiple input summing and subtracting amplifiers using the two-input summing amplifier as shown in Fig. 2.16 (a) are used as basic building blocks, it is possible to build

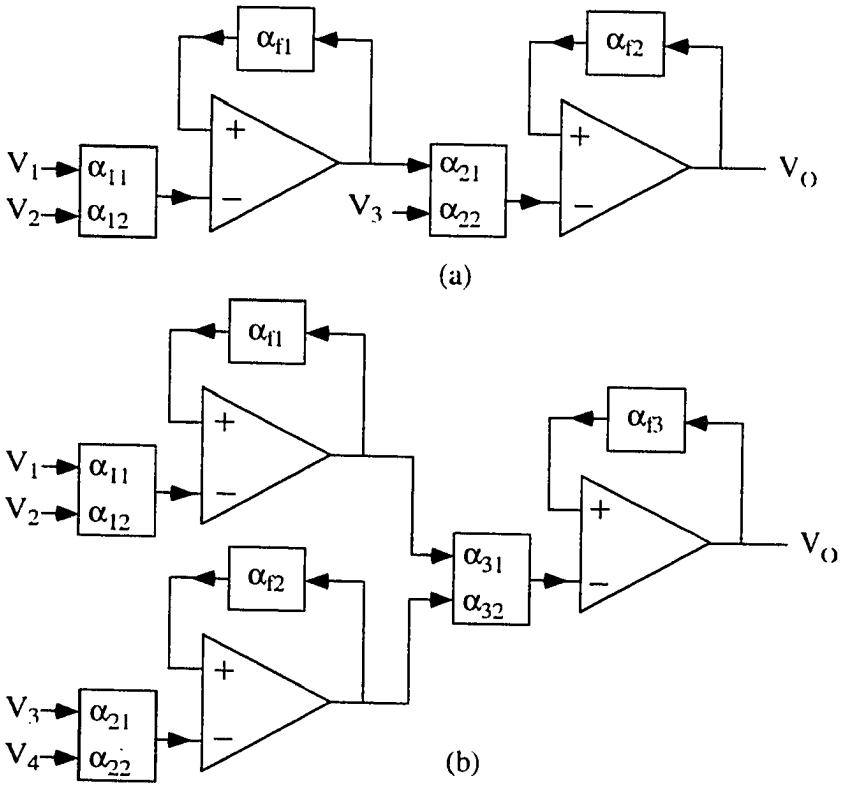


Figure 2.17: Examples of multiple input summing amplifiers

to build diverse summing/subtracting amplifiers. Thus, these multiple amplifiers will have more complicated versatile functions between the inputs and the output of the amplifiers.

2.7 Experimental Characterization

2.7.1 Experiments on attenuator I and amplifier employing it

MOSFETs of different sizes were fabricated using a standard 2μm CMOS process. Figure 2.18 shows the micrograph of the chip. The MOSFETs in the chip can be combined to form Attenuator I with a diverse attenuation factor. A lateral diffusion invariant layout scheme was used so the gains of the attenuator and amplifiers are not subject to the lateral diffusion of the drains and sources of the MOSFETs and the variation of the channel width. Figure 2.19 shows the measured dc transfer characteristic of the attenuator consisting of M1 (12μmx10μm) and M2 (3μmx10μm) when the substrate is common. V_{DD} was 5V in the measurement. The dc transfer characteristic exhibits a high degree of linearity for the input range of 2V to 5V. The small signal attenuation factor is 0.07824, measured by applying a 100mV (0-P) and 1kHz signal to the input at an input dc operating voltage of 3.5V. To further investigate the linearity of the attenuator, a sinusoidal input of 1kHz was applied at the 3.5V input dc operating voltage and the spectrum of the output was measured at different input amplitudes (0-P). The results are shown in Fig. 2.20. The signal to THD ratio was 76.0dB at 100mV (0-P) input signal amplitude and gradually decreased as the signal amplitude increased. . Using the noise model developed earlier, the output noise voltage was calculated as $1.1228 \times 10^{-5} V_{rms}$ for a noise band of 100Hz to 1mhz, the parameter values in Table 2.5, the dimensions of the

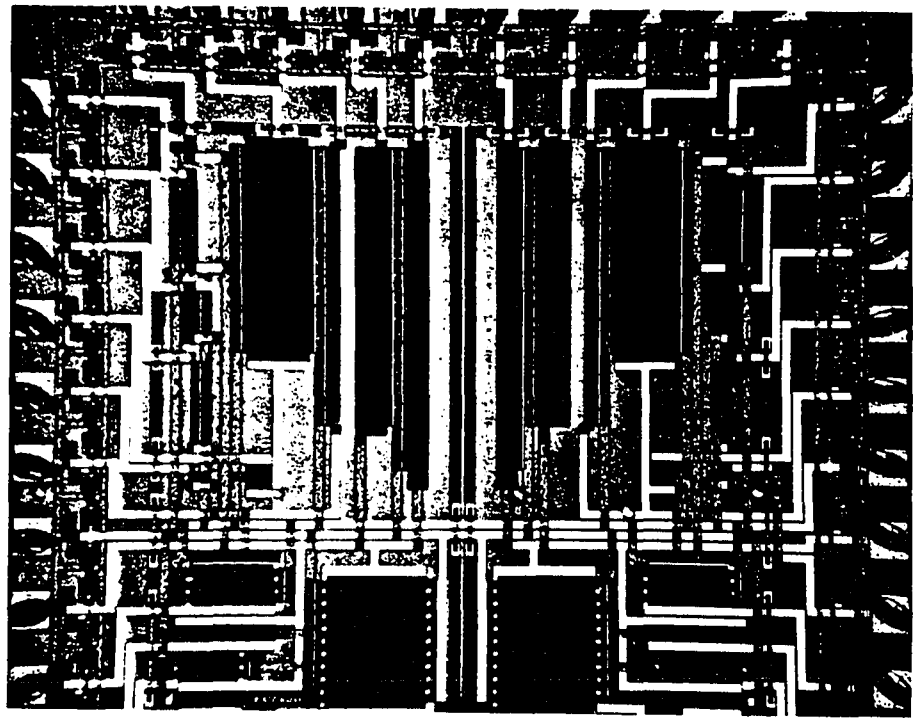


Figure 2.18: Chip micrograph

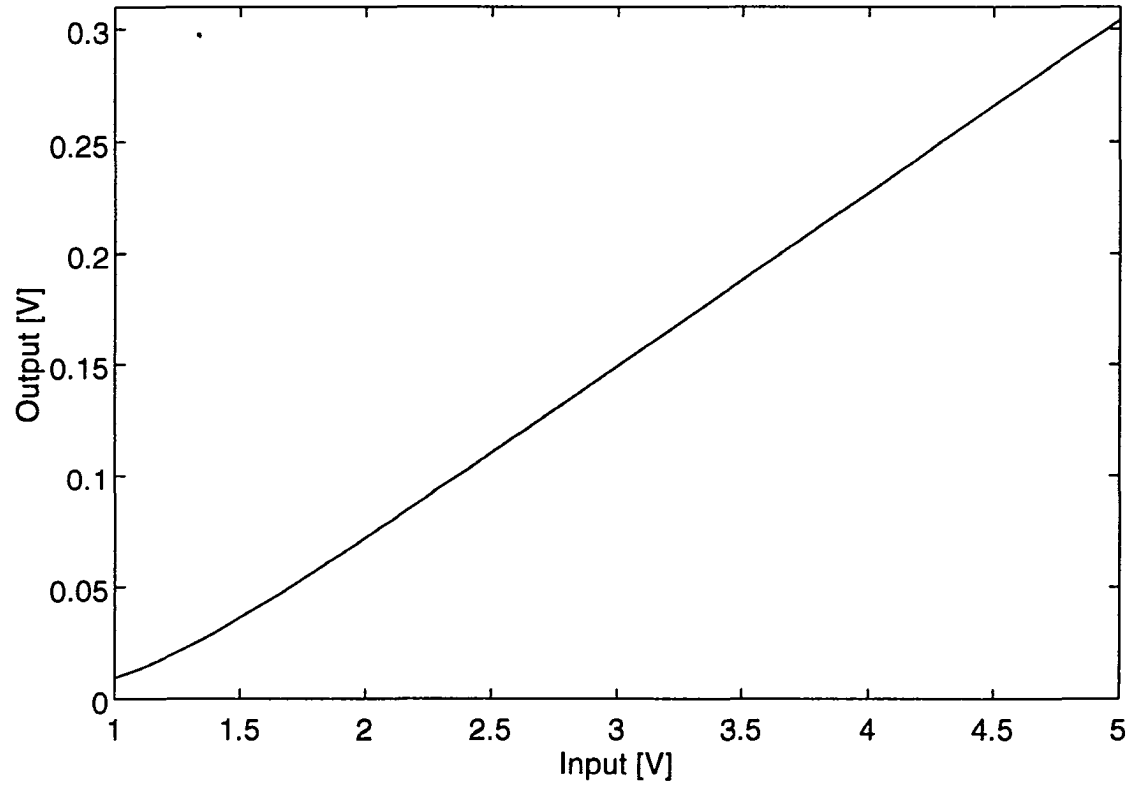


Figure 2.19: Measured dc transfer characteristic of Attenuator I

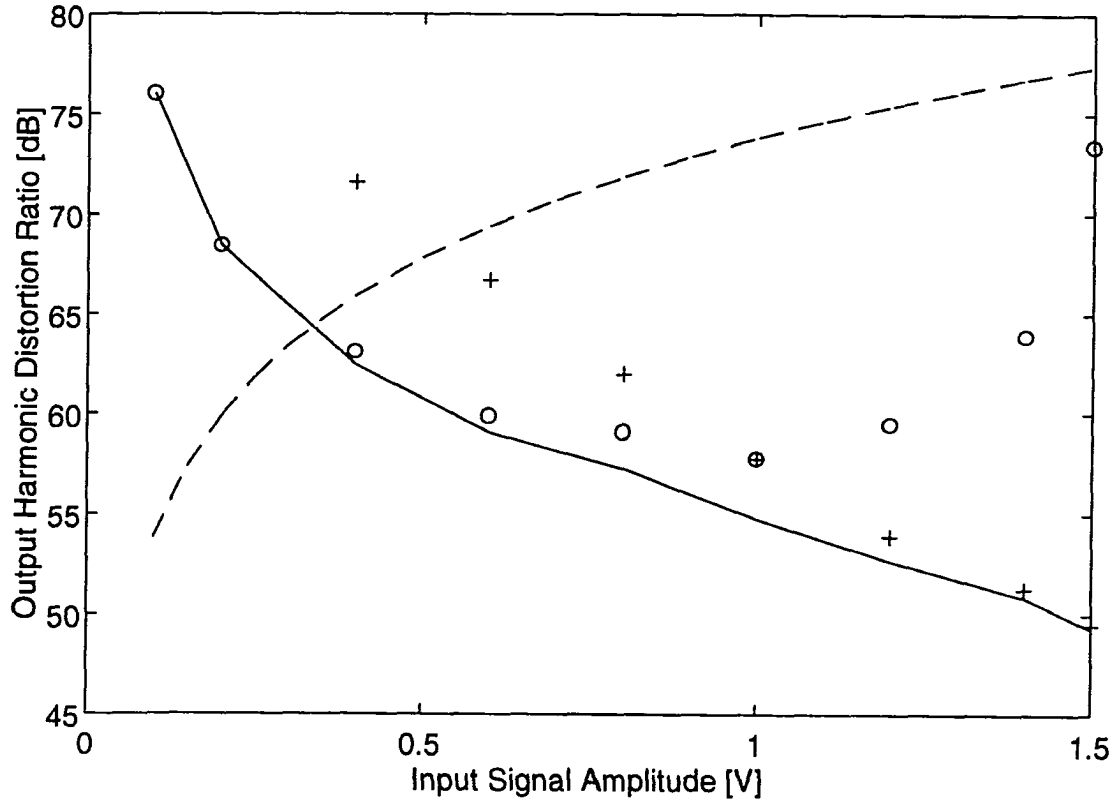


Figure 2.20: Measured signal to harmonic distortion ratios of the output of Attenuator I as a function of input amplitude (0-P): (__) signal to THD ratio, (o) signal to 2ndHD ratio, (+) signal to 3rdHD ratio, and (---) signal to noise ratio

MOSFETs, the dc operating voltages, and T=298K. The output signal to noise ratio is shown in Fig. 2.20 as a function of input signal amplitude (0-P). From Fig. 2.20, the maximum of the signal output to the total non-signal output ratio, STNR, is 61.2dB at an input signal amplitude of 330mV (0-P). The power consumption at the input dc operating voltage of 3.5V was measured as 185μW.

The amplifier shown in Fig. 2.5 was formed with the same attenuator characterized above and an LF351 op-amp. The measured dc transfer characteristic of the amplifier is shown in Fig. 2.21. The measured signal to THD ratio of the output, as a function of output amplitude (0-P) is shown in Fig. 2.22. The small signal gain at the 3.5V output dc operating voltage was measured as 12.72, when a 1kHz input signal was applied such that the output signal of the amplifier was 100mV. The signal to THD ratio of the output of the amplifier was 73.3dB at the output signal amplitude of 100mV with the output dc operating voltage at 3.5V. Neglecting the noise from the op-amp, the output noise voltage of the amplifier is the gain of the amplifier times the output noise voltage of the attenuator, that is, $1.4282\text{x}10^{-4}V_{rms}$. The calculated signal to noise ratio of the output of the amplifier as a function of the output amplitude (0-P), is also shown in Fig. 2.16. From Fig. 2.22, the STNR is 60.2dB, when the output signal amplitude is 290mV.

Table 2.5: Parameter set

parameter	value
V_{TON}	0.888 V
γ	1.0826 $V^{1/2}$
ϕ	0.6 V
K'	$4.3465\text{x}10^{-5}$ A/V^2
C_{ox}	$8.2414\text{x}10^{-4}$ F/m^2
K_f	$3\text{x}10^{-24}$ V^2F

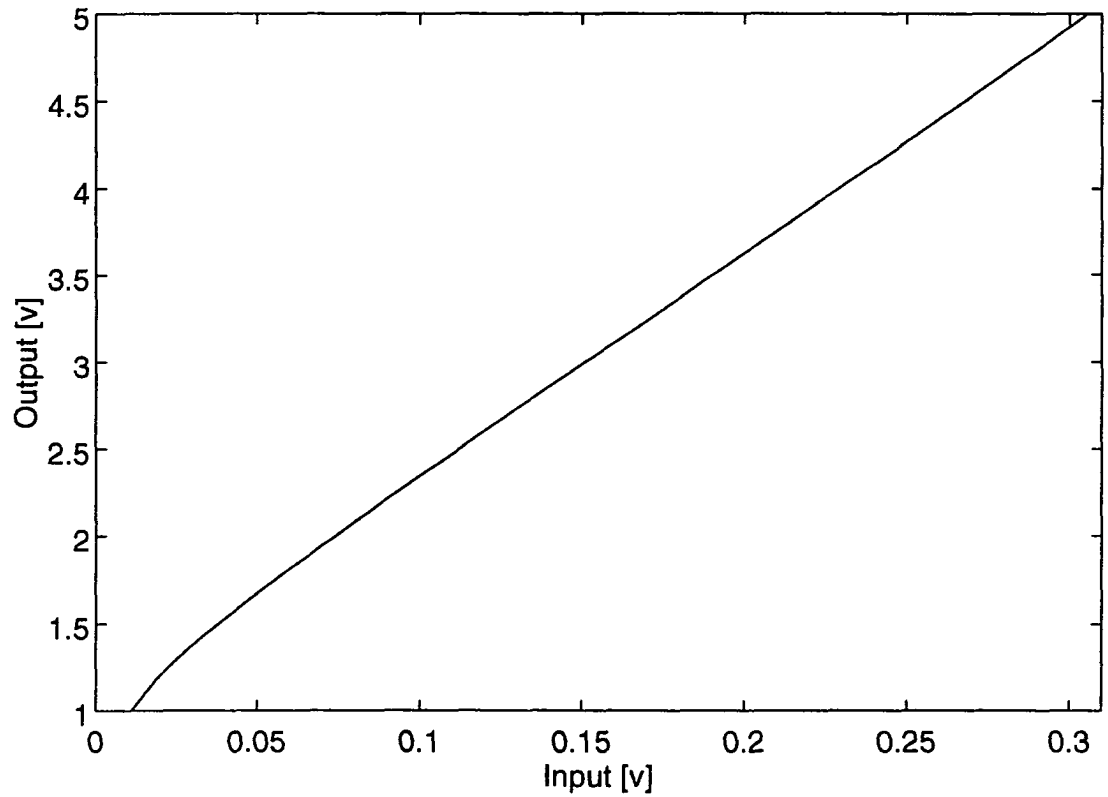


Figure 2.21: Measured dc transfer characteristic of the amplifier employing Attenuator I

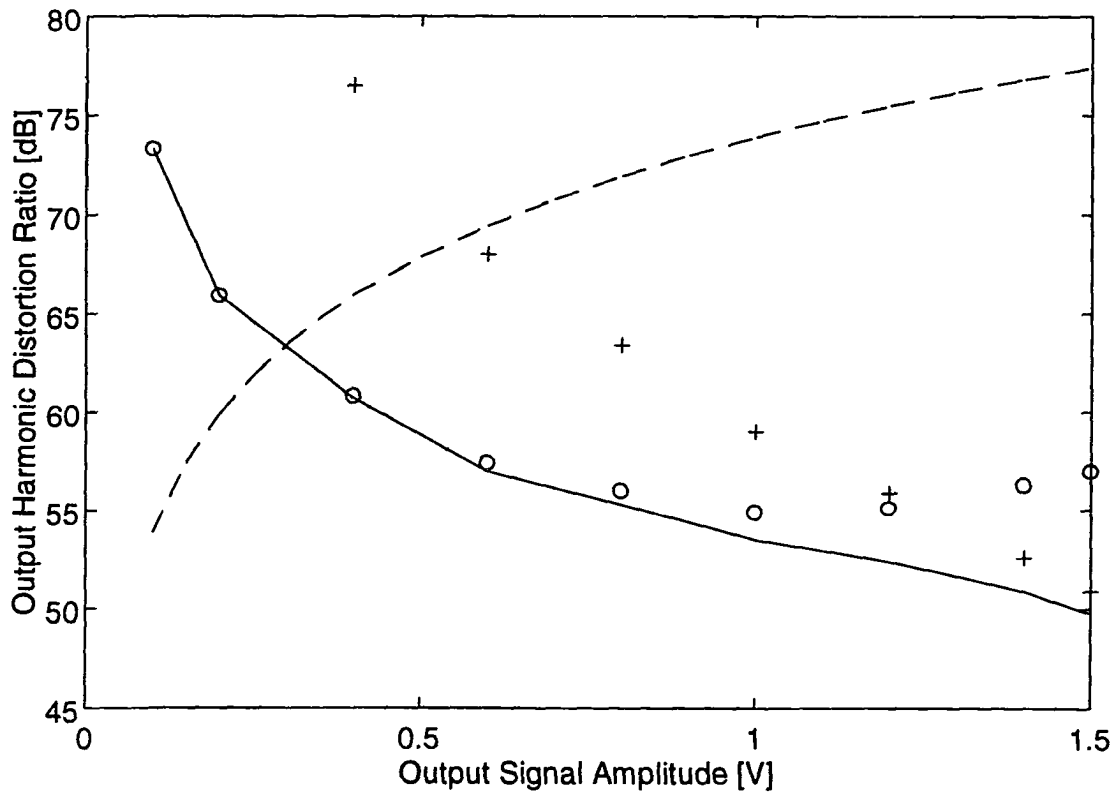


Figure 2.22: Measured signal to harmonic distortion ratios of the output of the amplifier as a function of output amplitude: (__) signal to THD ratio, (o) signal to 2ndHD ratio, (+) signal to 3rdHD ratio, and (---) signal to noise ratio

2.7.2 Experiments on Attenuator II, summing attenuator, and amplifier employing them

Attenuator II, summing attenuator, and the amplifiers employing them were fabricated in a standard 2μm CMOS process. Figures 2.23 and 2.24 show a microphotograph of the chips for the separate substrate case and common substrate case, respectively. The chips includes Attenuator II's, summing attenuators, amplifiers employing Attenuator I, summing amplifiers employing Attenuator II, and the summing amplifier and subtracting amplifiers employing Attenuator II and the summing attenuator.

The experimental results of the attenuators and amplifiers are presented. They were designed to achieve small signal gains in Tables 2.6 and 2.7. These attenuators and amplifiers were characterized by measuring small signal gain, dc transfer characteristics, and distortion spectrums of the outputs, by applying a 1kHz sinusoidal signal and the dc operating voltage. V_{DD} was 5V and the V_B and V_{BB} were set to the values shown in Tables 2.6 and 2.7 to have the output operating voltages as shown. The measured small signal gains are compared with the designed gain. The process-dependent parameters used are given in Table 2.8. The error between the measured and calculated gain ranges was 0.2-1.9% for the separate substrate cases and 2.1%-5.3% for the common substrate cases. Note, from Table 2.7 that the output operating voltage of the summing attenuator when the substrate was common and the threshold voltages of M4 and M2 were large was 1.884V, since it was impossible to raise it to 2.5V, the same as the input operating voltage. A further increase of V_{BB} to obtain the output operating voltage of 2.5V, forces M4 in the summing attenuator leave the saturation region. Even though the output operating voltage of the summing attenuator to cannot be equal to the input operating

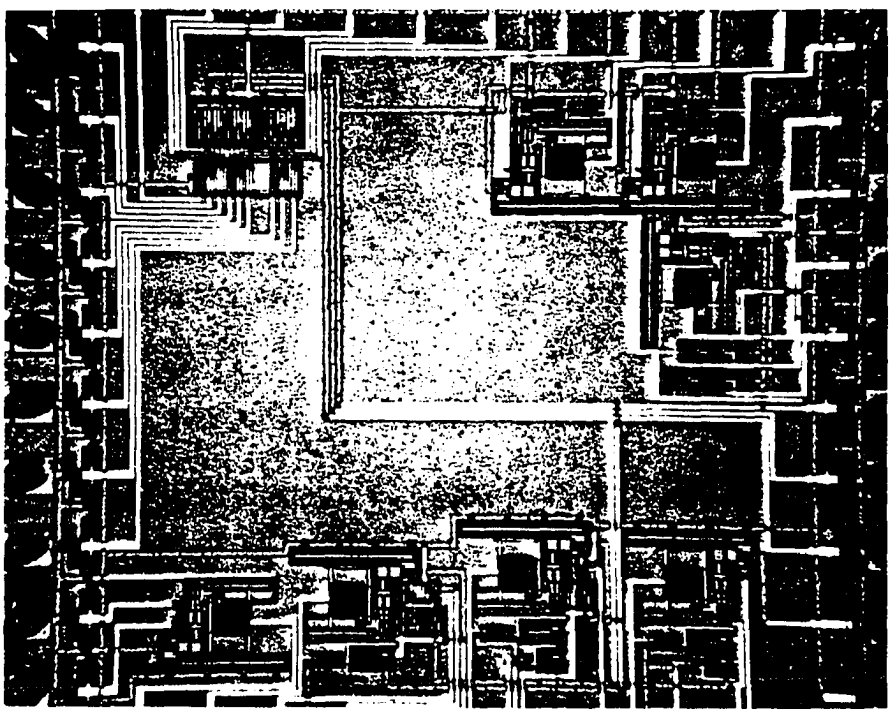


Figure 2.23: Chip micrograph, separate substrate

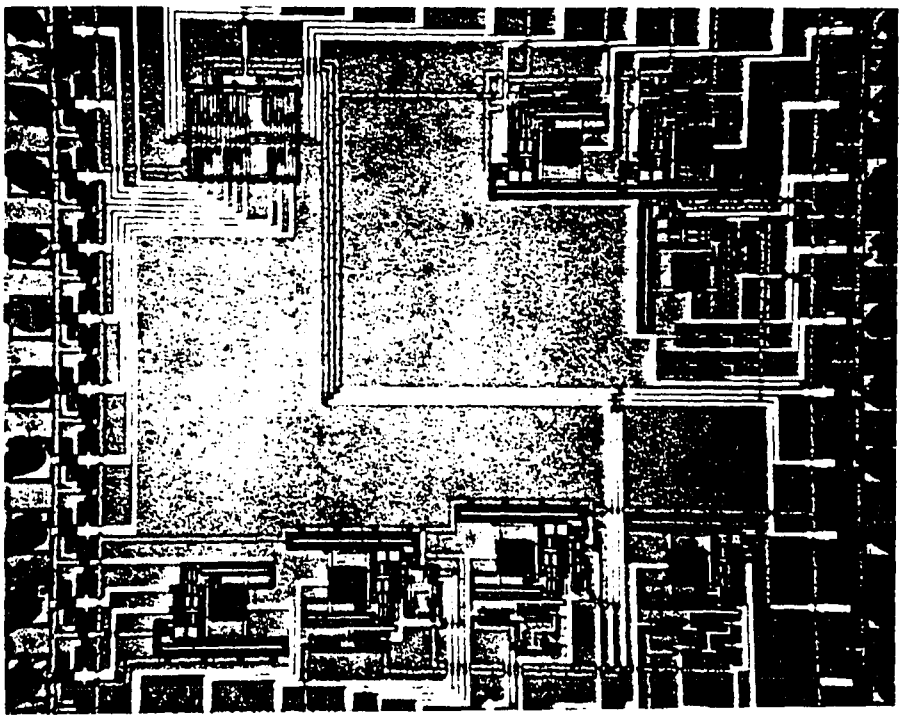


Figure 2.24: Chip micrograph, common substrate

Table 2.6: Bias voltage and comparison of simulated and measured gain, separate substrate case

	measured bias voltage [V]				small signal gain					
	operating vol.		V_B	V_{BB}	simulated		measured		error [%]	
	input	output			input 1	input 2	input 1	input 2	input 1	input 2
attenuator	2.5	2.5	3.732		-0.2357		-0.2330		1.14	
amplifier	2.5	2.5	3.736		-4.243		-4.273		0.71	
summing attenuator	2.5	2.5		4.984	-0.2357	-0.2357	-0.2337	-0.2352	0.85	0.22
summing amplifier	2.5	2.5	3.738	4.989	1	1	1.006	1.014	0.60	1.40
differential amplifier	2.5	2.5	2.231	3.476	1	-1	0.9807	-1.005	1.93	0.50

Table 2.7: Bias voltage and comparison of simulated and measured gain, common substrate case

	measured bias voltage [V]				small signal gain					
	operating vol.		V_B	V_{BB}	simulated		measured		error [%]	
	input	output			input 1	input 2	input 1	input 2	input 1	input 2
attenuator	2.5	2.5	5.221		-0.4221		-0.4035		4.42	
amplifier	2.5	2.5	5.225		-2.369		-2.466		4.12	
summing attenuator	2.5	1.884		7.669	-0.4092	-0.3174	-0.3933	-0.3266	3.89	2.92
summing amplifier	2.5	2.5	4.407	7.669	-0.9998	0.7753	0.9788	0.7928	2.10	2.25
differential amplifier	2.5	2.5	2.847	5.674	1.348	-1.349	1.280	1.277	5.07	5.32

Table 2.8: Parameter set

parameter	value	parameter	value
K'	4.471×10^{-5} A/V^2	L_D	0.2741 μm
C_{ox}	8.361×10^{-4} F/m^2	C_J	3.887×10^{-4} F/m^2
V_{TON}	0.8657 V	ϕ_B	0.8 V
γ	1.295 V$^{1/2}$	MJ	0.4466
ϕ	0.6 V	C_{JSW}	6.062×10^{-10} F/m
K_f	3×10^{-24} V^{2}F	$MJSW$	0.3269

voltage at 2.5V, it is still possible to make the amplifiers employing it have an output operating voltage of 2.5V. Thus, the output of the summing attenuator is always input to the op-amps forming the amplifiers. Note from Table 2.7 that when the substrate is common, the necessarily V_{BB} for the summing attenuators, which forms the summing amplifier and the differential amplifiers, are larger than V_{DD}. If the use of a power supply larger than V_{DD} needs to be avoided, a voltage shifter can be inserted between the attenuators, forming a summing attenuator to reduce the necessary V_{BB}. With the voltage shifter between attenuators, it is possible to construct a multiple input (more than 2) summing attenuator with a finite voltage for V_{BB}.

Figures 2.25-2.34 show the measured dc transfer characteristics of the attenuators, amplifiers, and the output distortions as a function of the input amplitude (0-P) for the attenuators and as a function of output amplitude (0-P) for the amplifiers. For the summing amplifiers, the distortions are shown as a function of the output amplitude (0-P) due to input 1. In the distortion spectrum measurements, the 10Hz sinusoidal signal was applied for the first input and 13Hz sinusoidal signal was applied for the second input (if any) at 2.5V dc voltage. The output spectrums at different inputs (for the attenuators) or output amplitudes (for the amplifiers) were measured. Using the models developed earlier,

the signal to noise ratios were calculated for the parameter values in Table 2.8, a noise band of 100Hz-1MHz, and T=298K. The results are shown along with the measured signal to distortion ratios as a function of signal amplitude (0-P) in Fig. 2.25-2.34.

Table 2.9 summarizes the performances of the attenuators and amplifiers tested. It lists the calculated output noise voltage, signal to total distortion ratio at 100mV (0-P) (input amplitude for the attenuators and output amplitude for the amplifiers), STNR using the calculated output noise and measured signal to total distortions, and the signal amplitude (0-P) (input amplitude for the attenuators and output amplitude due to V_1 for the amplifiers) for the maximum output signal to non-signal output ratio.

In these experiments, the dimensions of the attenuators were W_1=W_3=6μm, L_1=L_3=8μm, W_2=W_4=108μm and L_2=L_4=8μm for all separate substrate cases, and W_1=W_3=6μm, L_1=L_3=8μm, W_2=W_4=18μm and L_2=L_4=8μm for all common substrate cases. A lateral diffusion invariant layout scheme was used so the gains of the attenuator and amplifiers are not subject to the lateral diffusion of the drains and sources of the MOSFETs.

In general, spectrum measurements showed that when the dimensions of the MOSFETs forming the attenuators are the same, the signal to distortion ratios for the separate substrate case were 1-2dB better than those for the common substrate case. This slightly better performance of the separate substrate case is attributed to the fact that, if the dimensions are the same, the attenuator with a separate substrate has a slightly larger attenuation factor. Thus, the attenuator with a larger gain showed a better linearity. Besides attenuators with separate substrates have an advantage over the attenuators with a common substrate. We can more precisely control the attenuation factor of the attenuator with a separate substrate independent of the process parameters. If the dimensions of the MOSFETs forming the attenuator are the same, the linearity performance of the attenua-

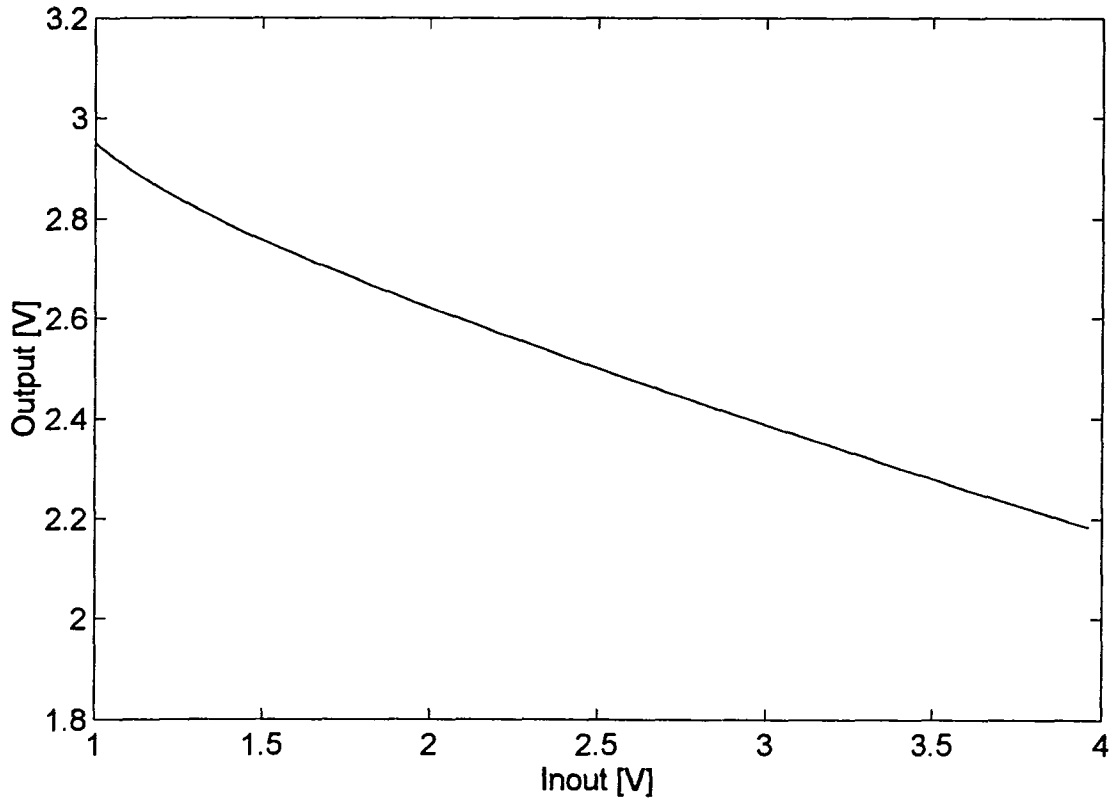


Figure 2.25: Measured characteristic of Attenuator II, separate substrate:
(a) dc transfer characteristic,

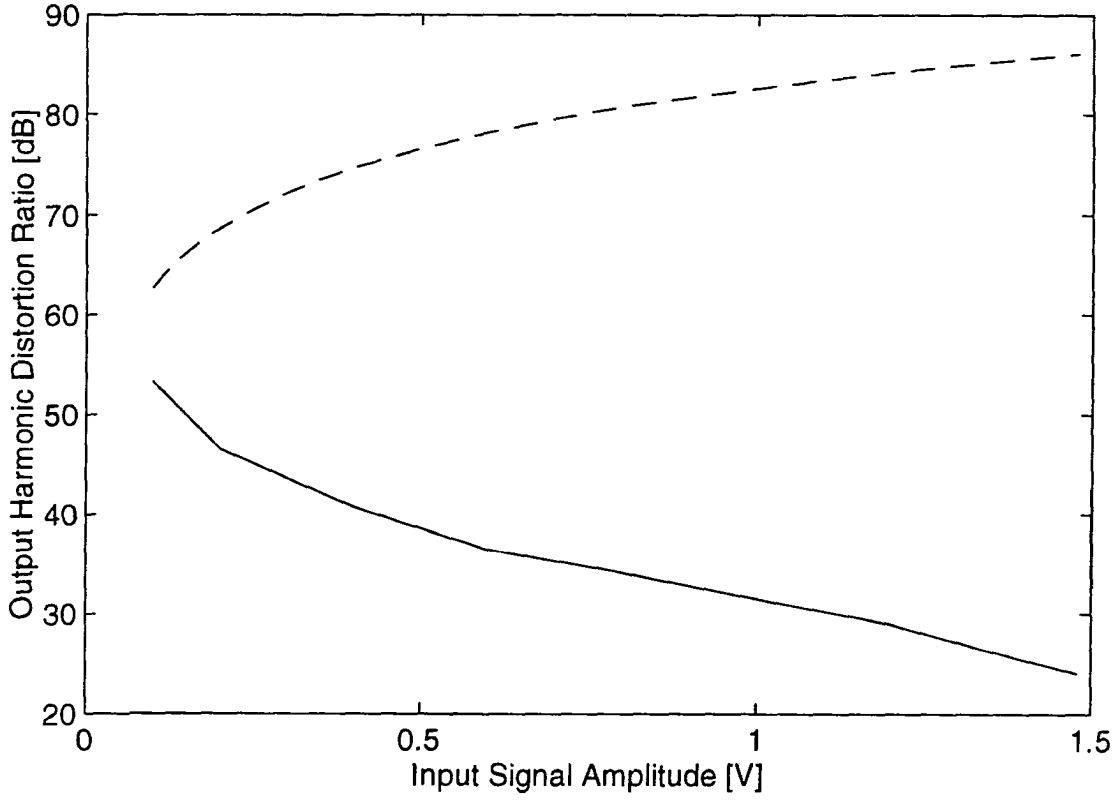


Figure 2.25: (continued) (b) Output distortion: (__) signal to THD ratio, (---) signal to noise ratio

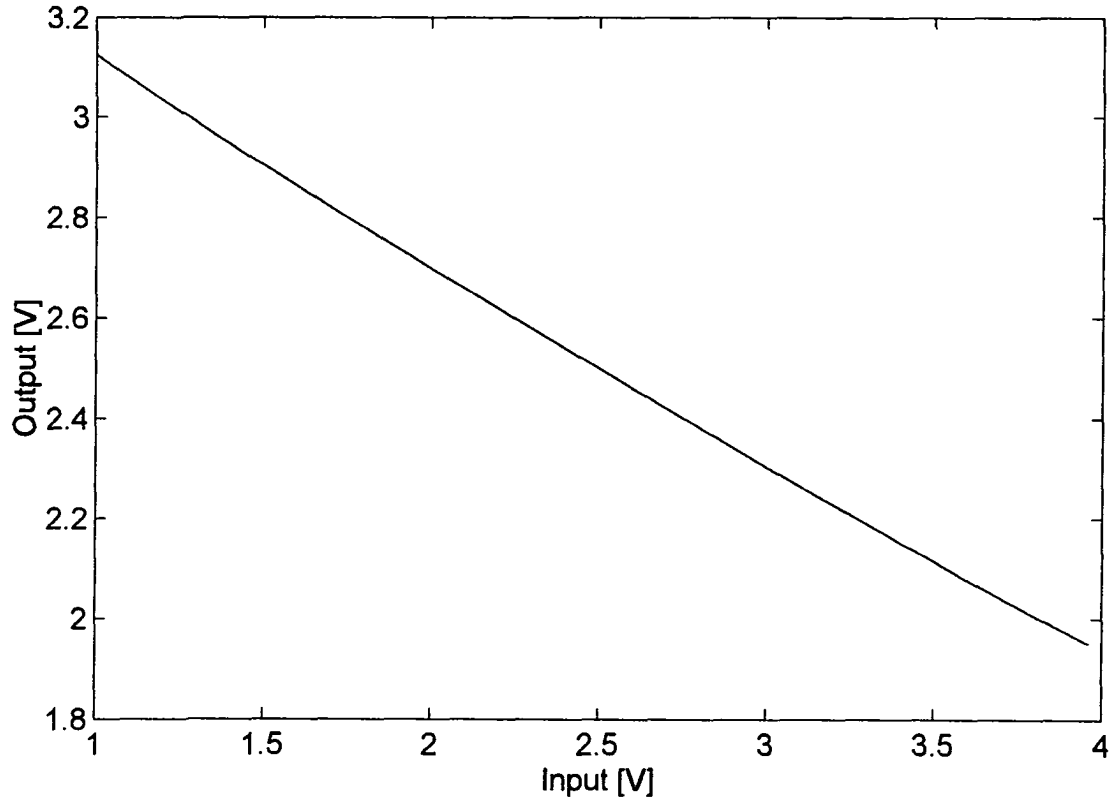


Figure 2.26: Measured characteristic of Attenuator II, common substrate: (a) dc transfer characteristic,

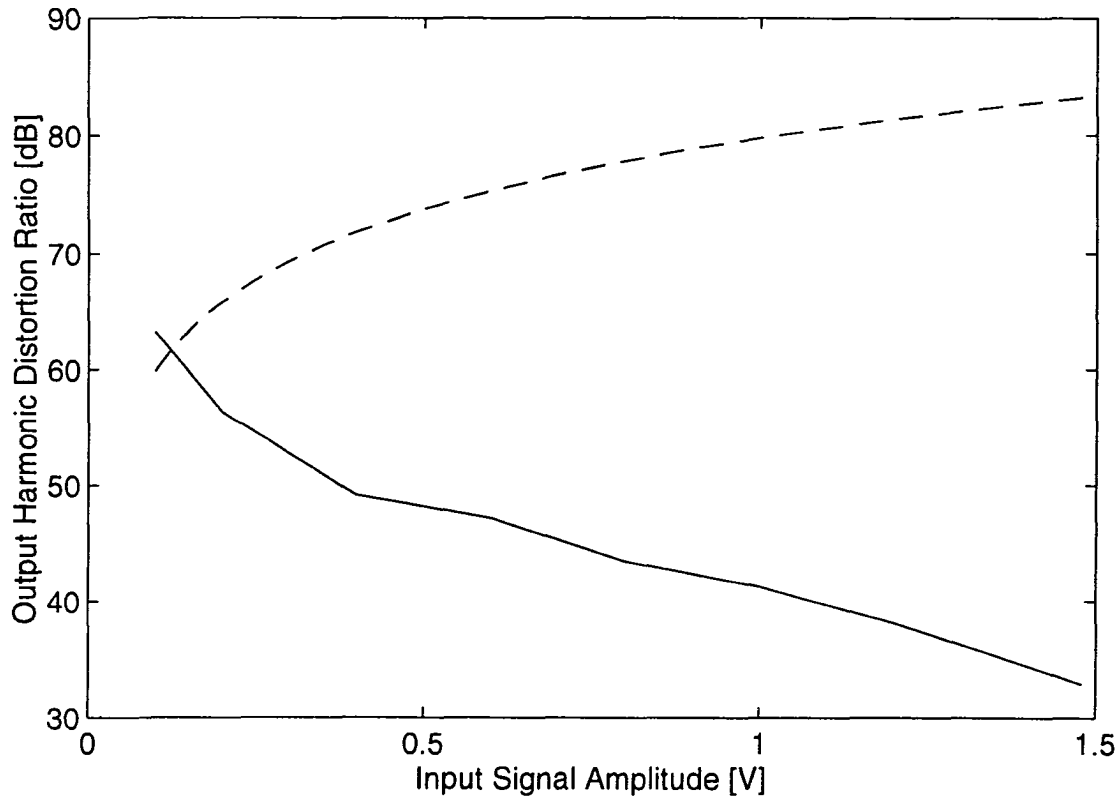


Figure 2.26: (continued) (b) Output distortion: (__) signal to THD ratio, (---) signal to noise ratio

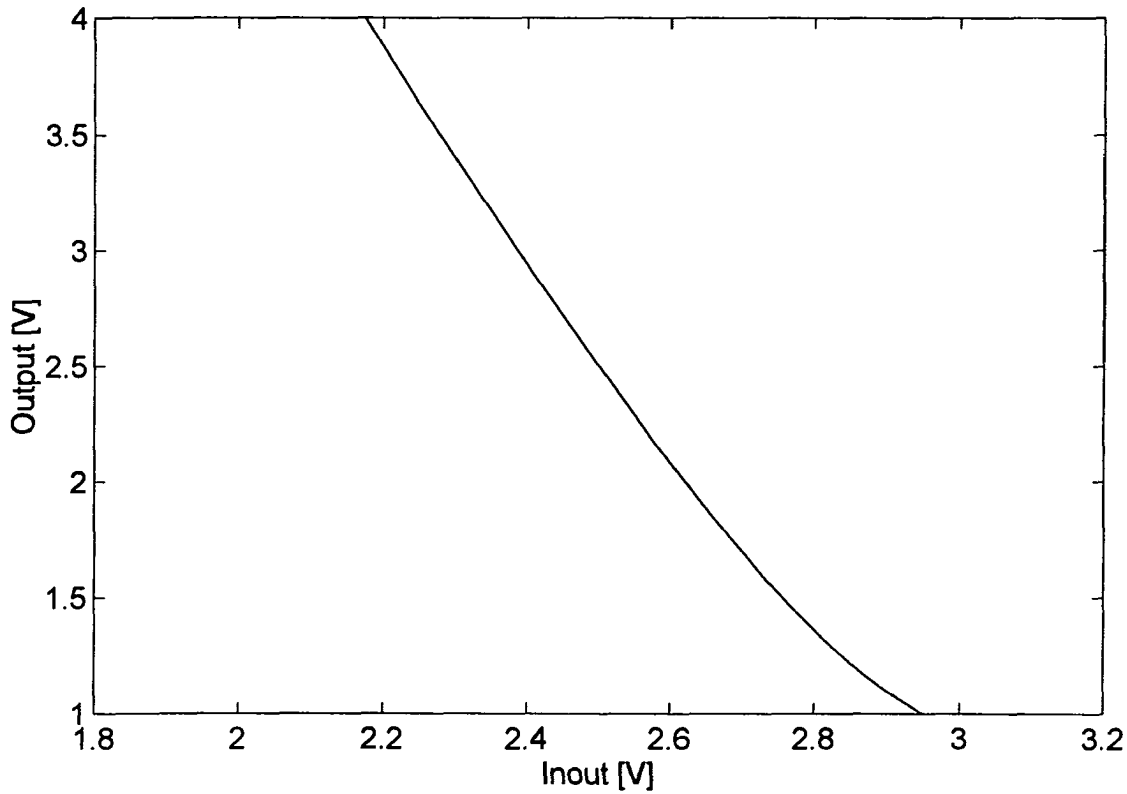


Figure 2.27: Measured characteristic of amplifier employing Attenuator II, separate substrate: (a) dc transfer characteristic,

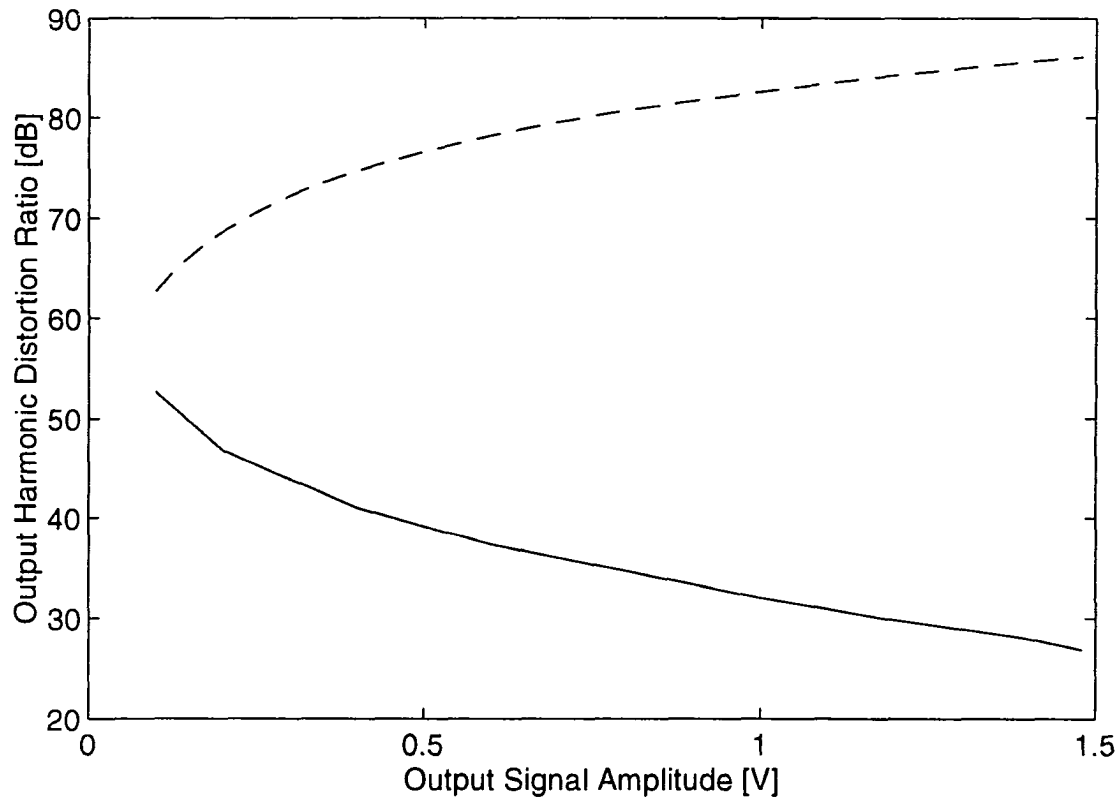


Figure 2.27: (continued) (b) Output distortion: (__) signal to THD ratio, (---) signal to noise ratio

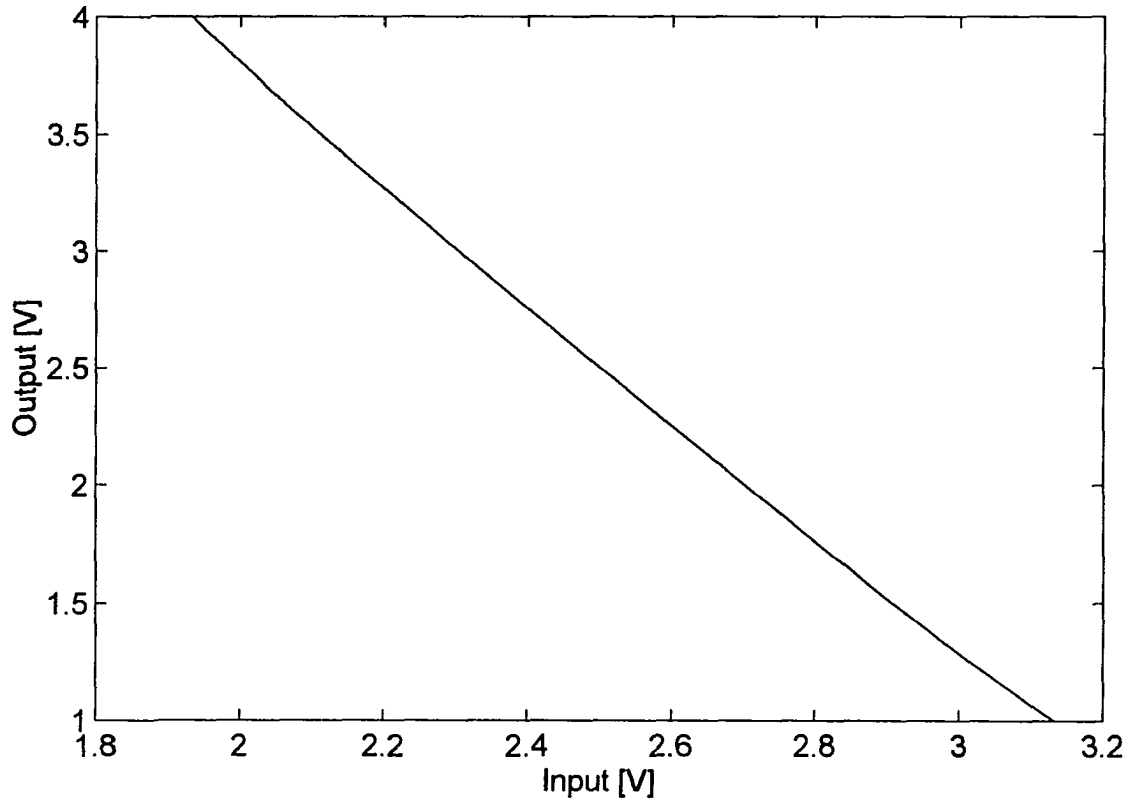


Figure 2.28: Measured characteristic of amplifier employing Attenuator II, common substrate: (a) dc transfer characteristic,

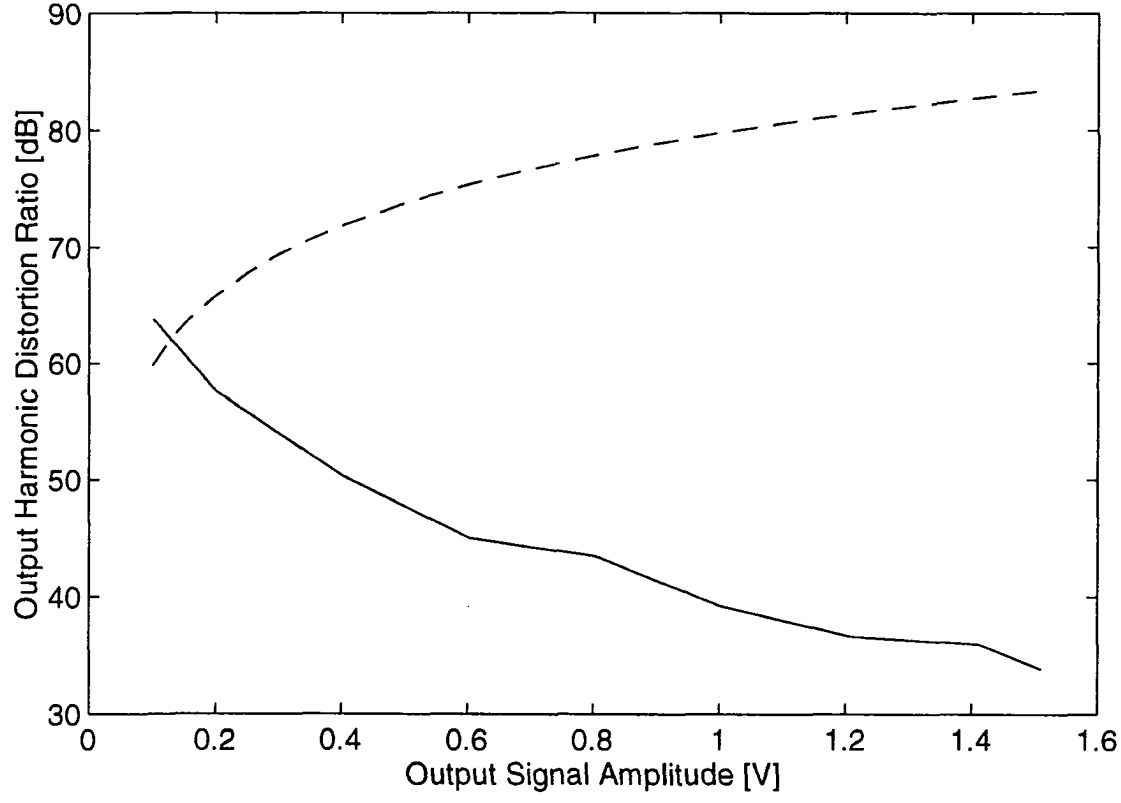


Figure 2.28: (continued) (b) Output distortion: (__) signal to THD ratio, (---) signal to noise ratio

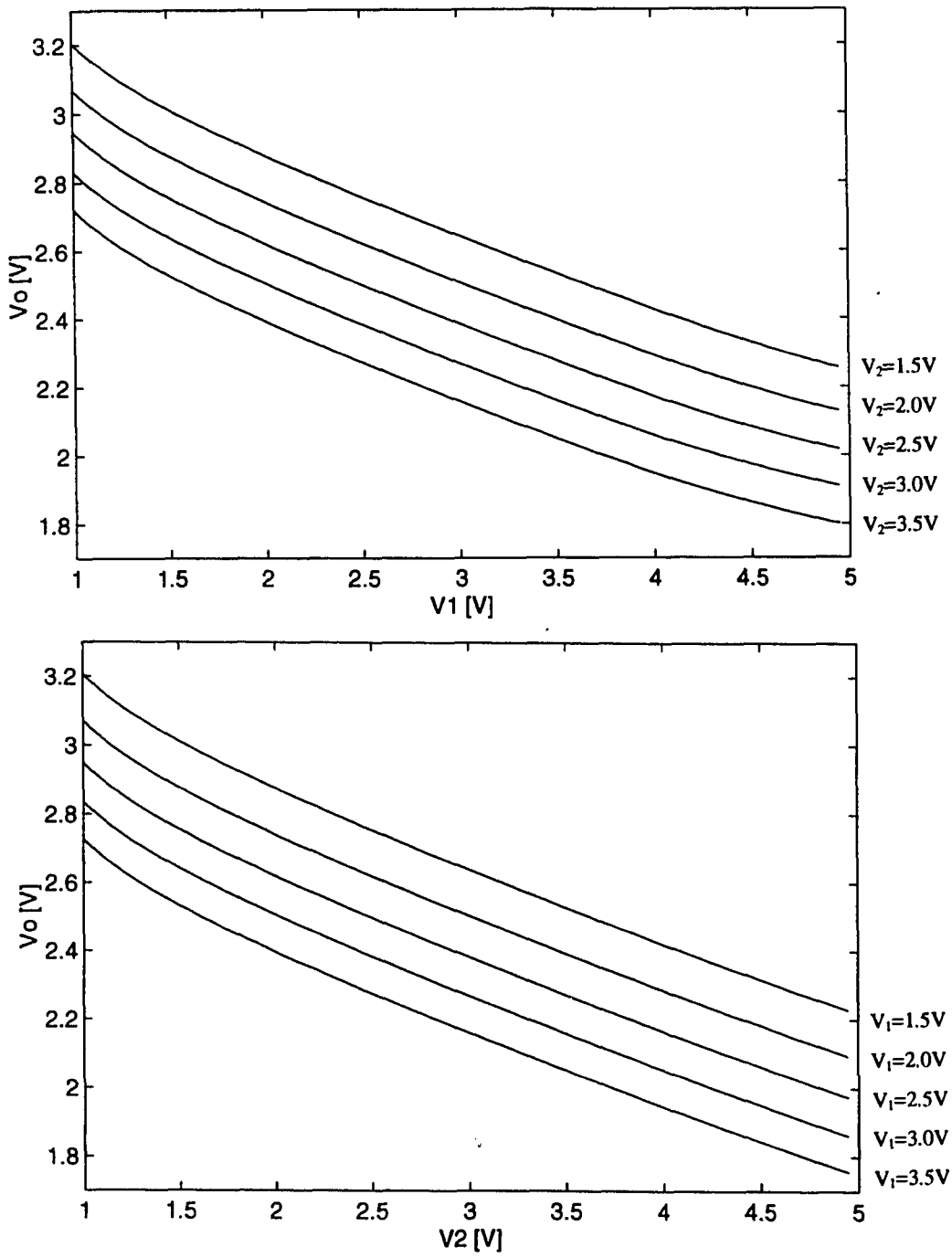


Figure 2.29: Measured characteristic of summing attenuator, separate substrate: (a) dc transfer characteristic,

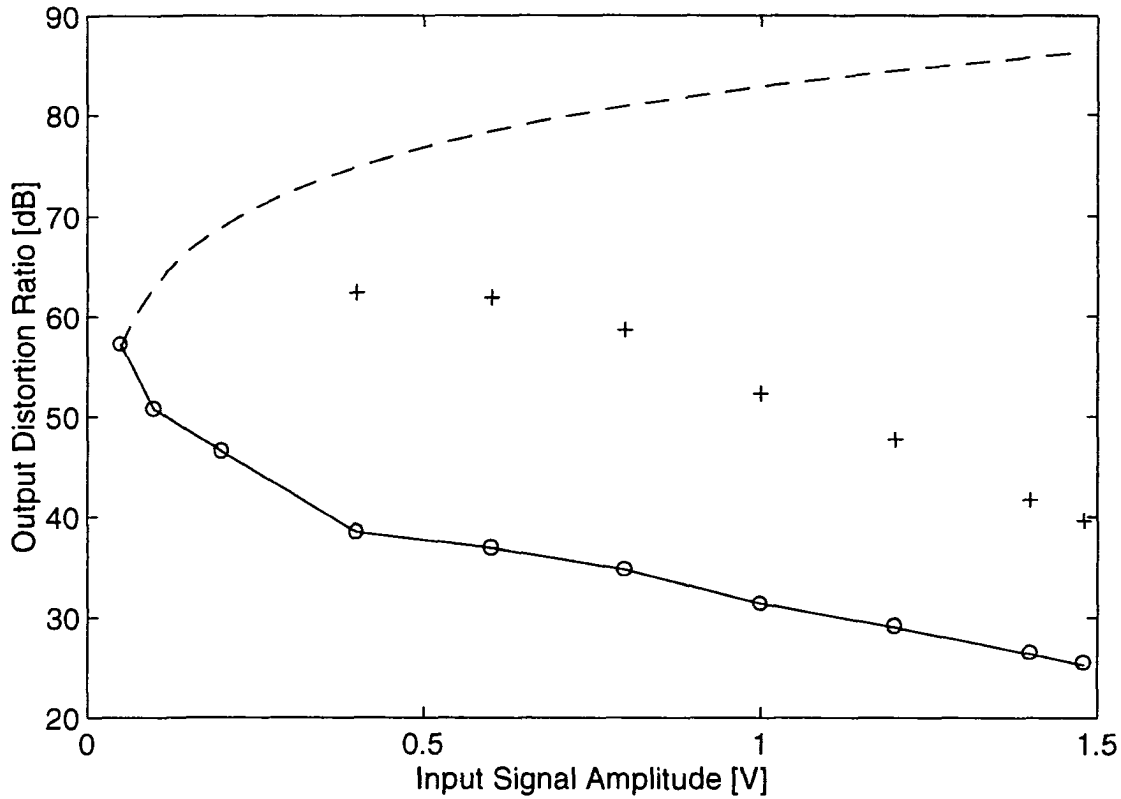


Figure 2.29: (continued) (b) Output distortion: (__) signal to TD ratio, (o) signal to THD ratio, (+) signal to TID ratio, (---) signal to noise ratio

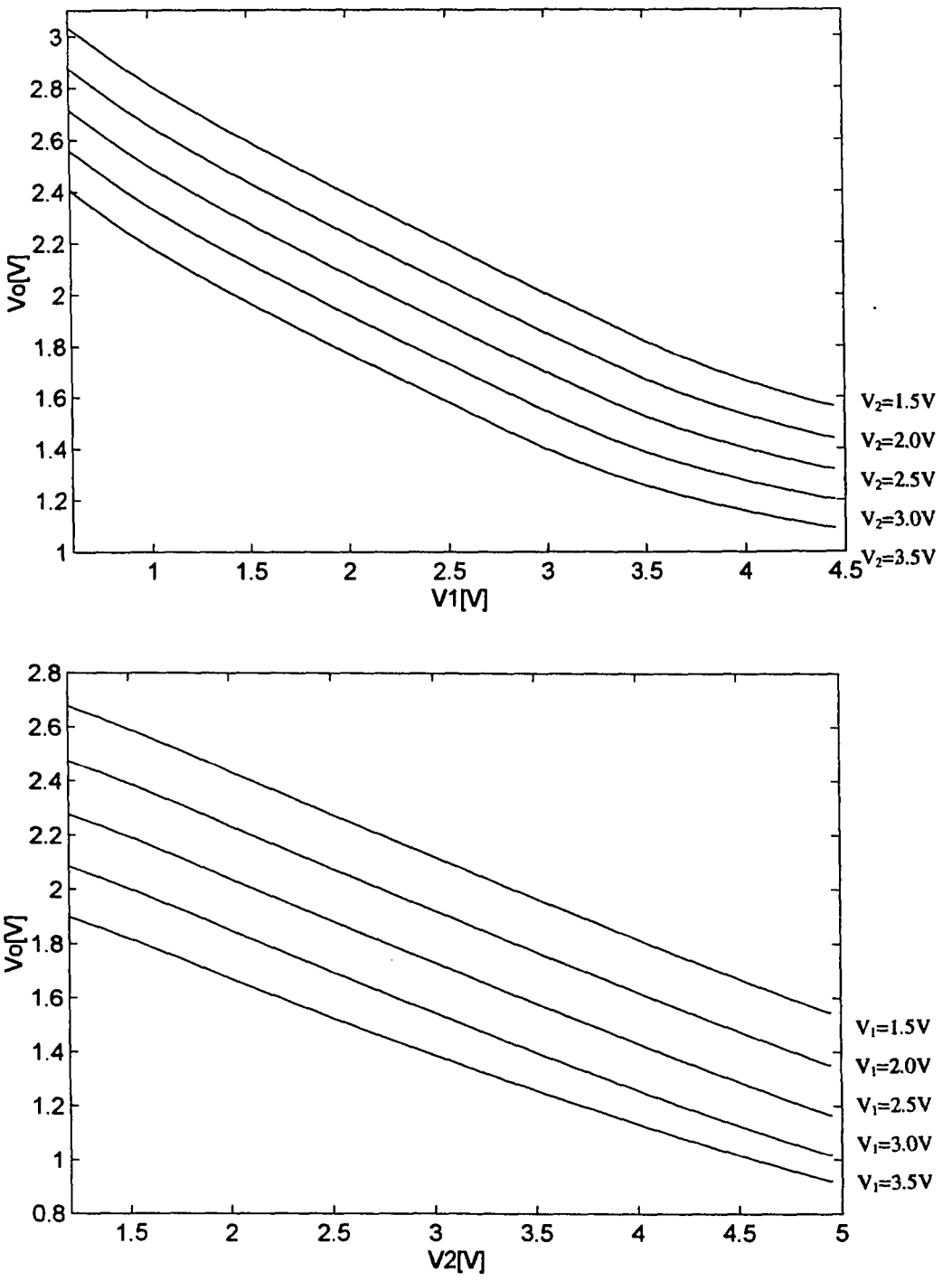


Figure 2.30: Measured characteristic of summing attenuator, common substrate: (a) dc transfer characteristic,

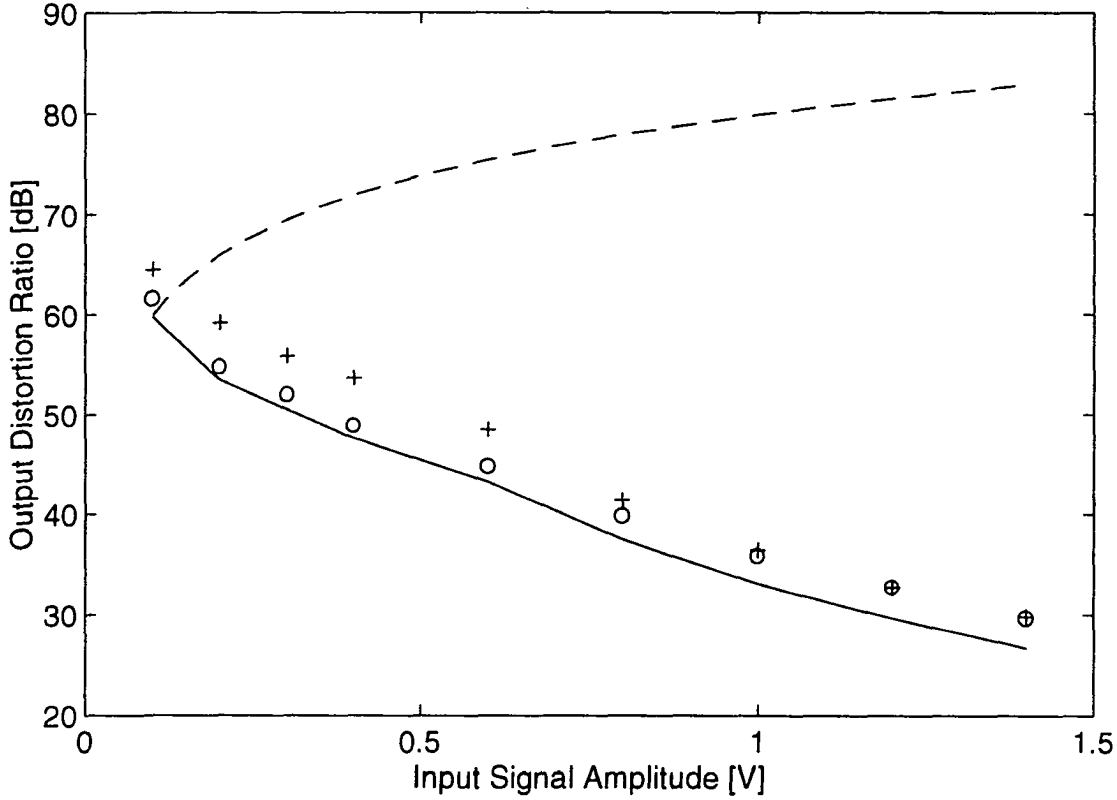


Figure 2.30: (continued) (b) Output distortion: (__) signal to TD ratio, (o) signal to THD ratio, (+) signal to TID ratio, (---) signal to noise ratio

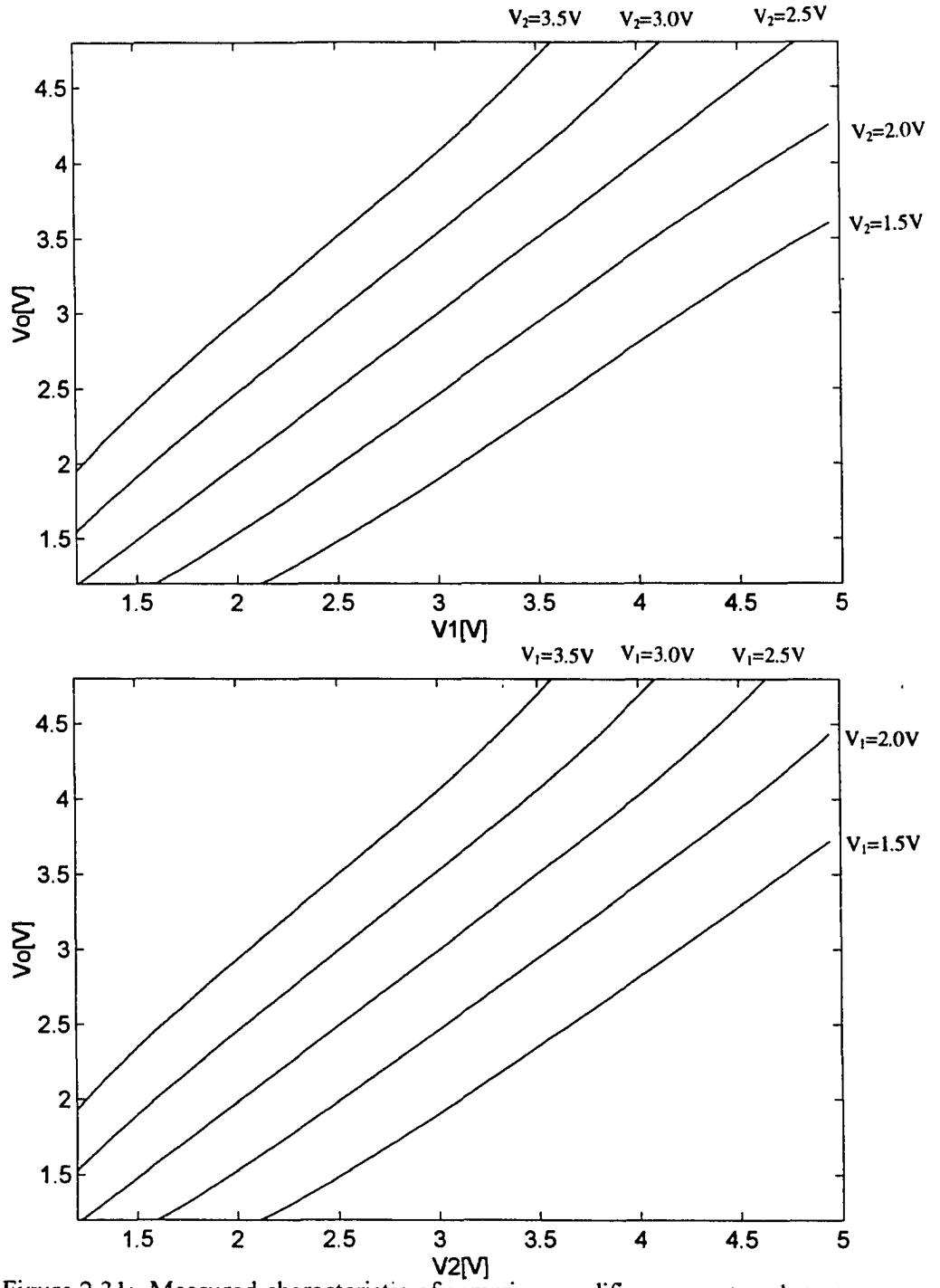


Figure 2.31: Measured characteristic of summing amplifier, separate substrate: (a) dc transfer characteristic,

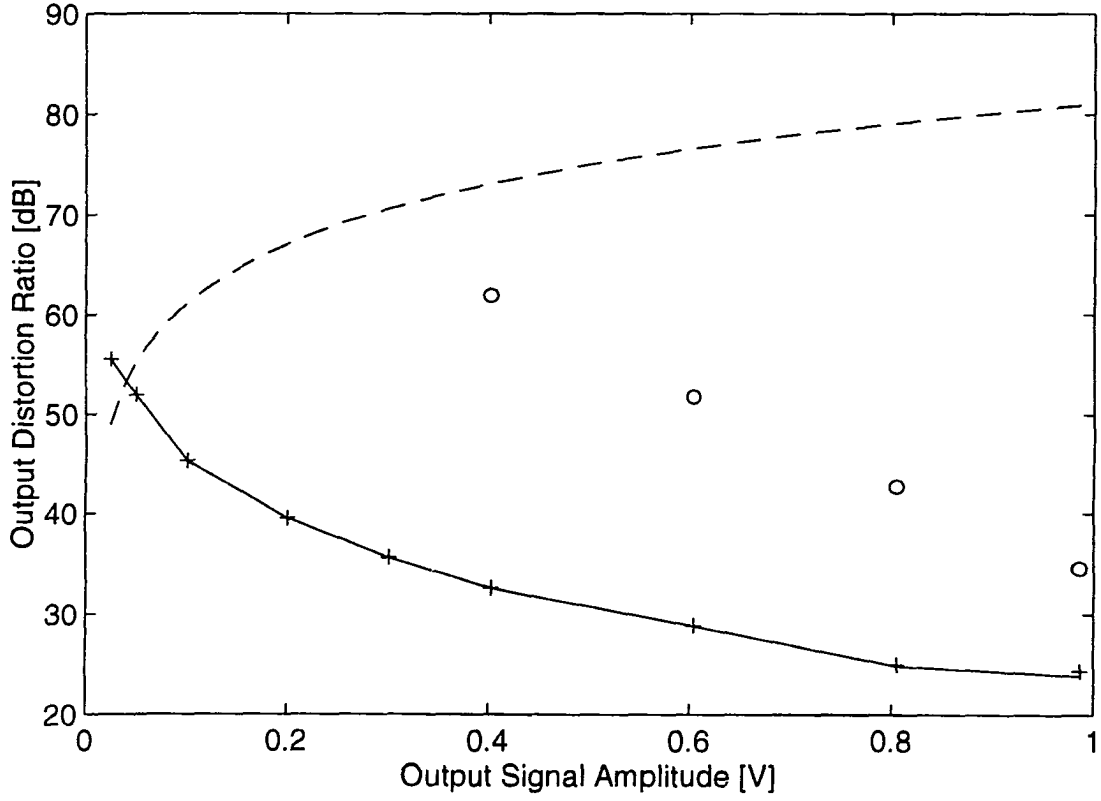


Figure 2.31: (continued) (b) Output distortion: (__) signal to TD ratio, (o) signal to THD ratio, (+) signal to TID ratio, (---) signal to noise ratio

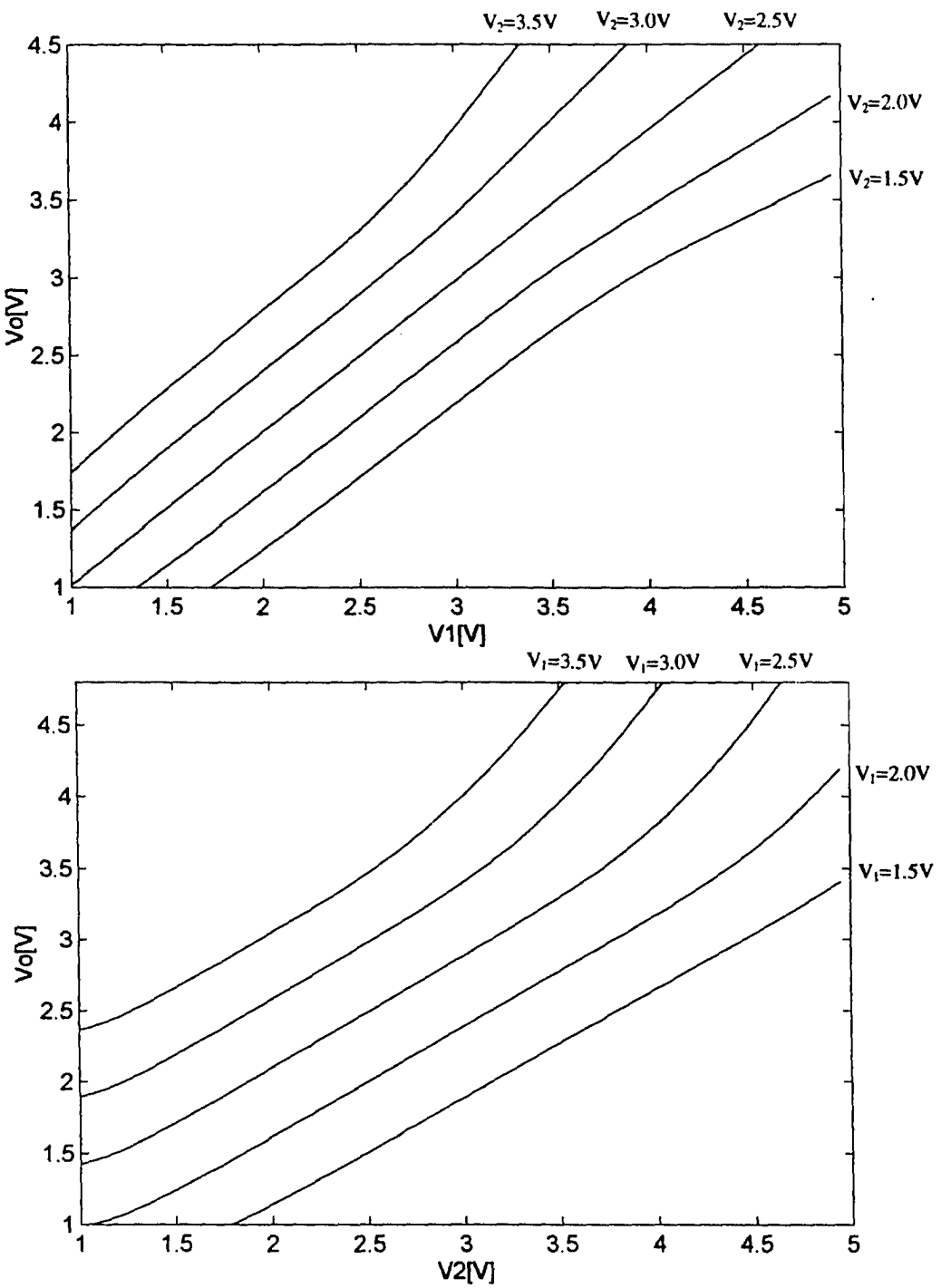


Figure 2.32: Measured characteristic of summing amplifier, common substrate: (a) dc transfer characteristic,

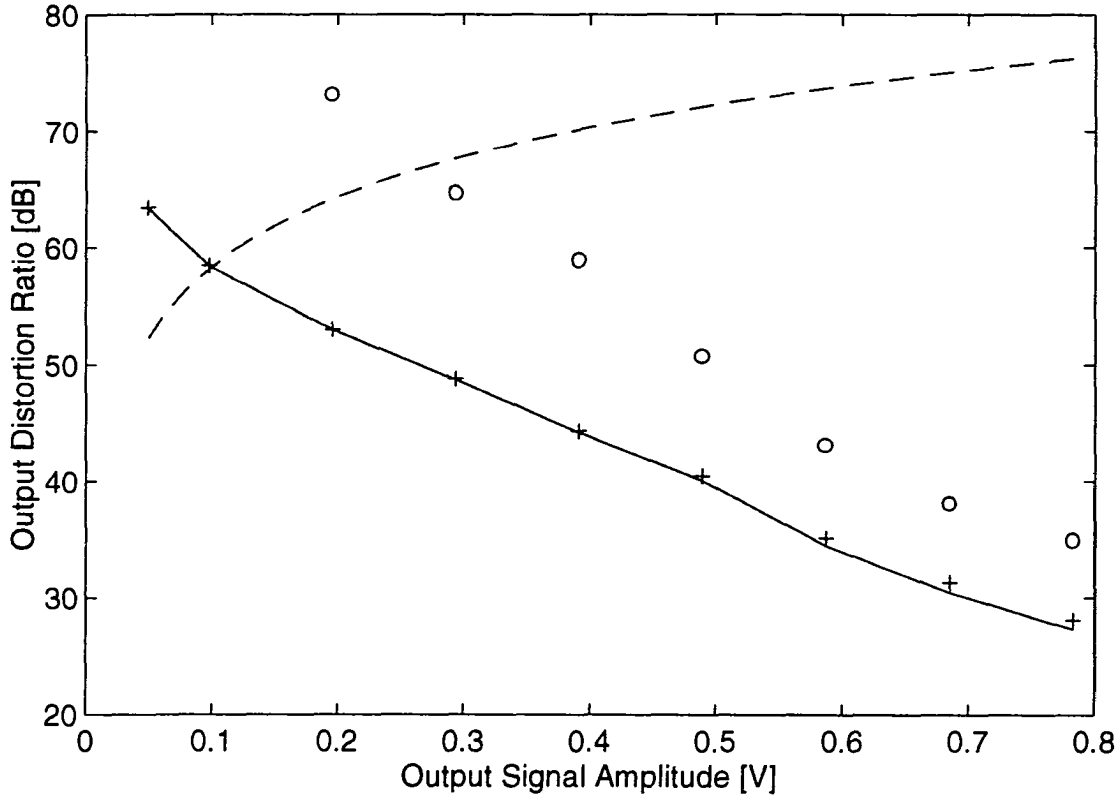


Figure 2.32: (continued) (b) Output distortion: (__) signal to TD ratio, (o) signal to THD ratio, (+) signal to TID ratio, (---) signal to noise ratio

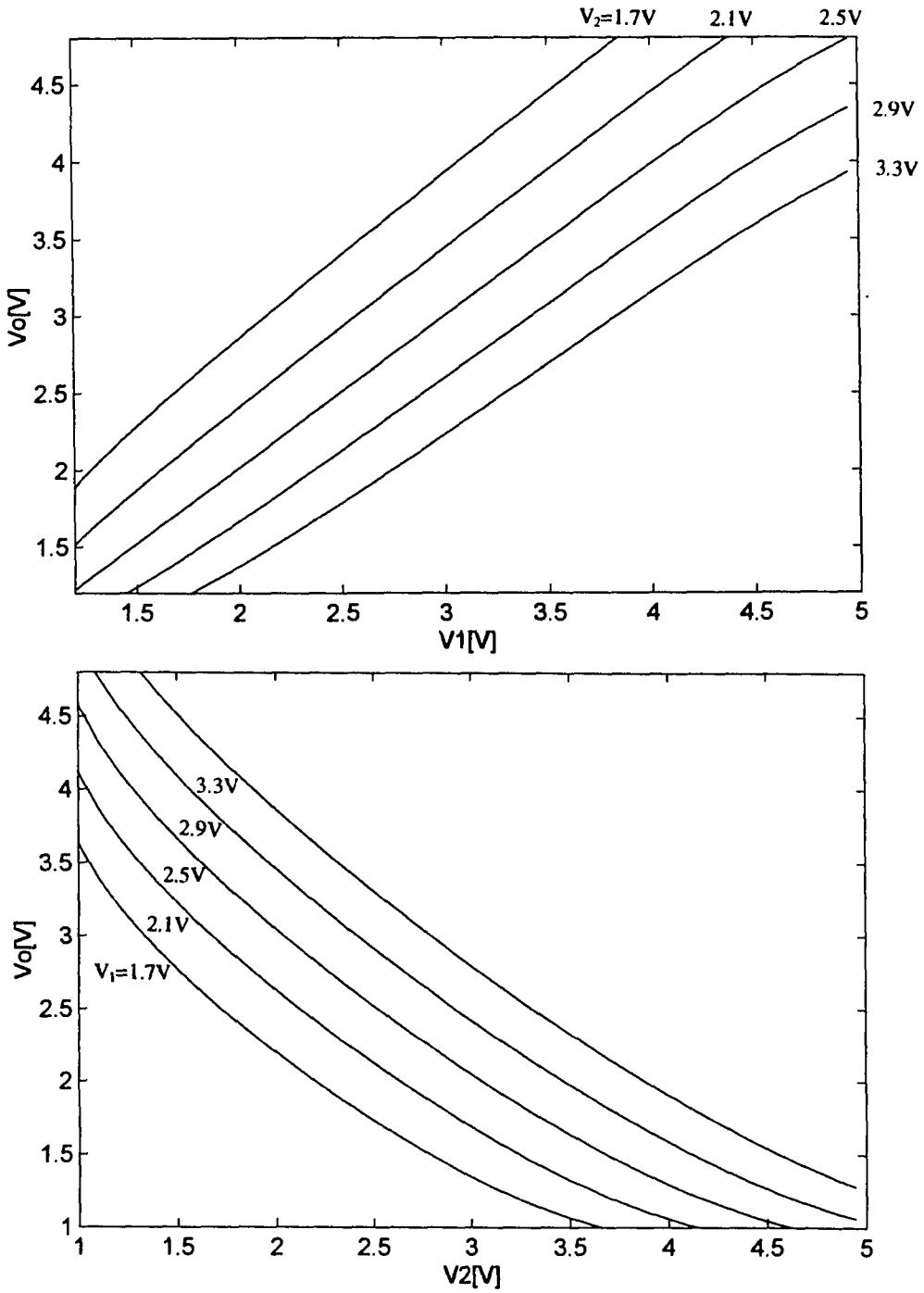


Figure 2.33: Measured characteristic of subtracting amplifier, separate substrate: (a) dc transfer characteristic,

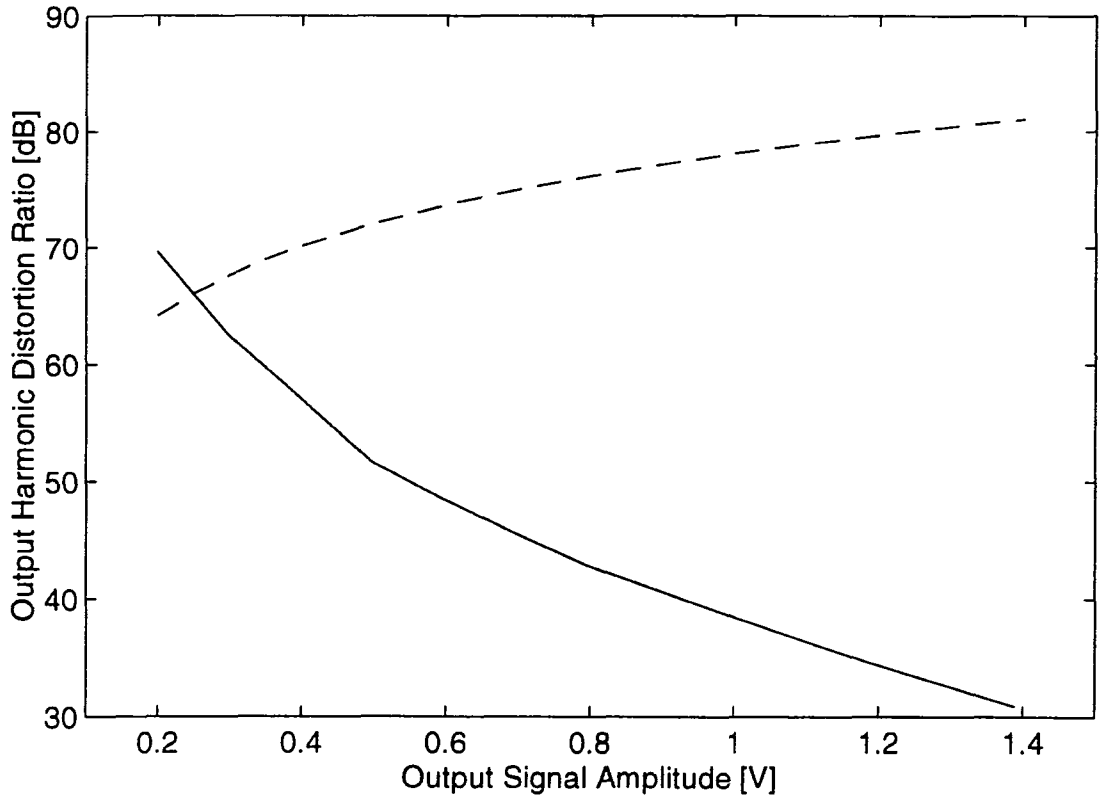


Figure 2.33: (continued) (b) Output distortion: (__) signal to THD ratio, (---) signal to noise ratio

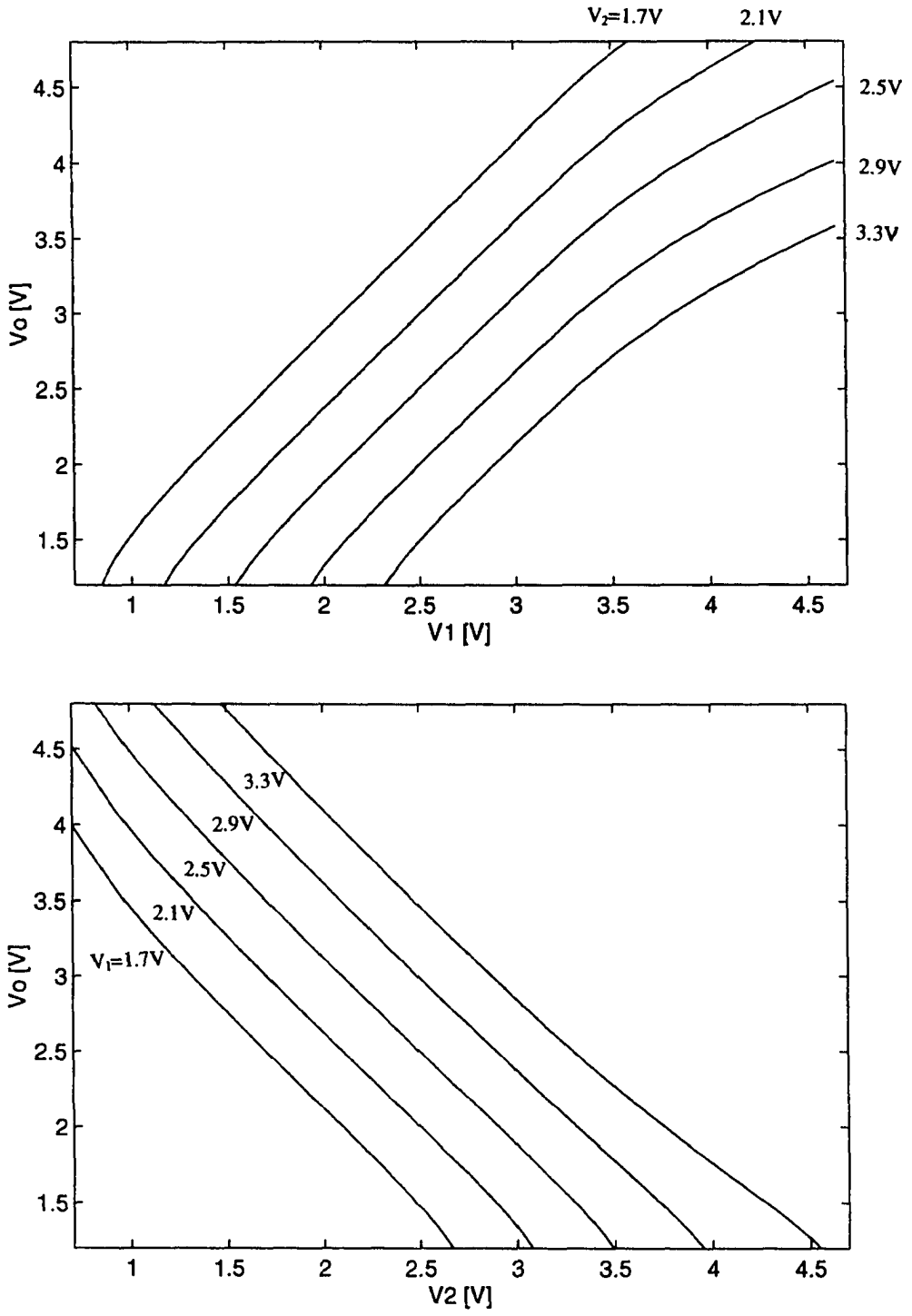


Figure 2.34: Measured characteristic of subtracting amplifier, common substrate: (a) dc transfer characteristic,

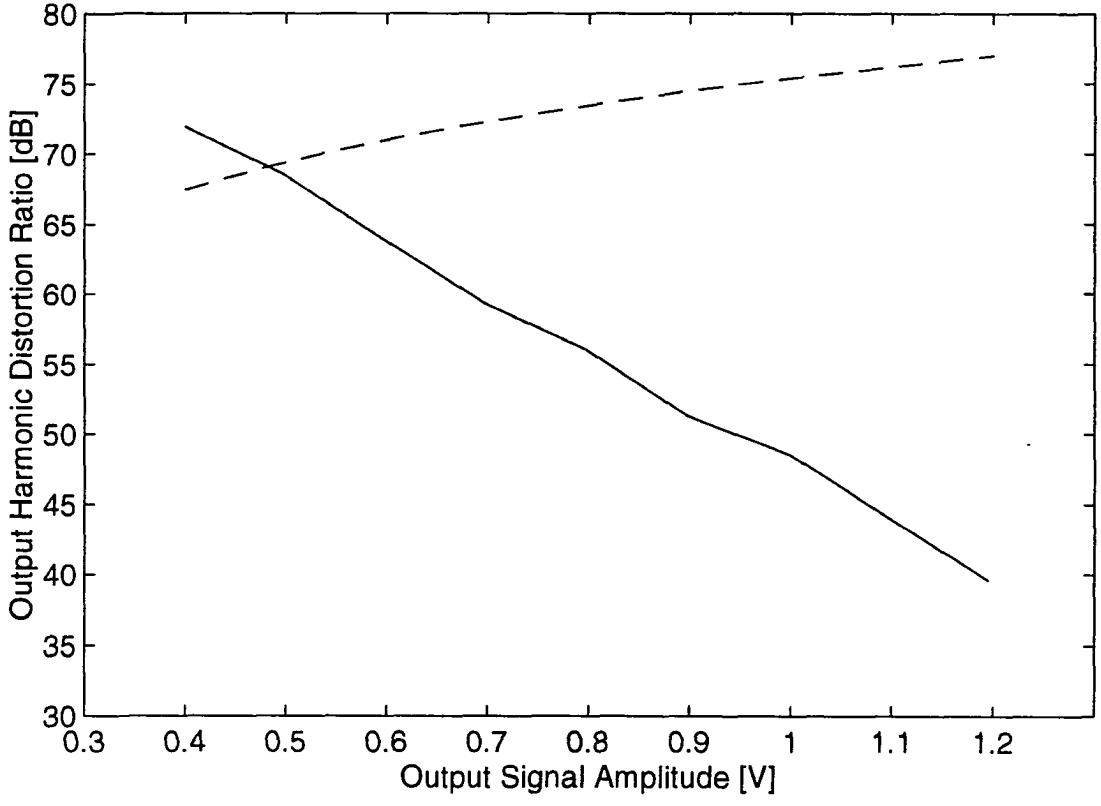


Figure 2.34: (continued) (b) Output distortion: (__) signal to THD ratio, (---) signal to noise ratio

Table 2.9: Attenuator/Amplifier performance summary

	$R_1 = R_2 = 0.2357$ Separate Substrate				$R_1 = R_2 = 0.5774$ Common Substrate			
	output noise [μV_{rms}]	S/TD at 100mV (0-P) [dB]	output STNR [dB]	optimal sig. amp (0-P) [mV]	output noise [μV_{rms}]	S/TD at 100mV (0-P) [dB]	output STNR [dB]	optimal sig. amp (0-P) [mV]
attenuator	12.12	53.3	55.1	57.2	29.17	63.2	58.6	123
amplifier	51.99	52.6	54.1	56.5	72.44	63.8	58.9	129
summing attenuator	16.78	50.8	54.1	49.7	36.4	59.8	56.7	98.7
summing amplifier	88.69	45.3	50.3	40.7	110.2	58.4	55.0	98.6
differential amplifier	87.88	>70	63.1	249	119.7	>80	66.2	482

tors and amplifiers are similar when the substrates are separate and when the substrates are common. The experimentally characterized performance of the attenuators and amplifiers when R is small (R=0.2357) was shown with the separate substrate cases, and the performance when R is large (R=0.5573) was shown with the common substrate case.

2.8 Conclusions

Versatile finite gain amplifiers especially suitable for monolithic applications were presented. The versatile finite gain amplifiers were realized by employing active voltage attenuators consisting of MOSFETs in the feedback path of an operational amplifier. The attenuators included two different types of single input attenuators and a summing attenuator evolved from one of the single attenuators. The summing attenuator is expandable to multiple input summing attenuators. The amplifiers realizable with the attenuators and operation amplifiers are two different kinds of single input finite gain amplifiers, a summing amplifier and a differential or subtracting amplifier. Combining the amplifiers, it is possible to construct multiple input summing/subtracting amplifiers. The attenuators and amplifiers were analyzed for the dc transfer characteristics, harmonic and intermodulation distortions, output noise voltage, and frequency response. The design methods of the attenuators for minimum noise or for minimum power consumption were discussed. The simulation results using the analyses were presented. The actual performance of the attenuators and amplifiers were characterized with experiments. In the experiments, the linearity and the range of the linear region of the attenuators and amplifiers were first characterized by measuring the dc transfer characteristics. Then, the accuracy of the gains of the attenuators and amplifiers was verified by comparing the measured gains with the simulated gains using the models developed. Finally, the degree

of linearity as a function of the input or output voltage range was characterized by measuring the harmonic and intermodulation distortions as a function of the input or output amplitude.

The active attenuators have many attractive characteristics, including a small size, nearly infinite input impedance, low power consumption, and offset adjustability independent of the attenuation ratio. It is believed that attenuators with these merits and the versatile finite gain amplifiers realized with the attenuators should find applications in mixed-signal integrated circuits.

CHAPTER 3. A CHARGE CONSERVING MACROMODEL FOR MOSFETS

3.1 Introduction

In this chapter, a charge conserving macromodel for MOSFETs suitable for simulating the charge injection behavior of MOSFET switches is presented. In analog and mixed-signal MOS integrated circuits, switches designed to exploit the inherent switching characteristics of MOSFETs have been widely used. The circuits are descriptively termed as MOS switches. The major limitation of the MOSFET switch is that it disturbs the adjacent node voltages when it is turned off. The disturbance is due to two factors, injection of the channel charge in the switching transistor when the MOSFET switch is turned off, and coupling through the gate-drain/source overlap capacitances. These non-idealities, which are often described as clock-feed-through (CLFT) effects, degrade the performance of circuits using MOSFET switches.

This non-ideal behavior of the MOSFET switch and techniques to compensate the disturbances have been investigated [13-20]. Models for MOSFETs that can be used to simulate the charge injection behavior have been developed [21-30]. The nature of the models is summarized in Table 3.1. The models in [21, 23] are a 50-50 split lumped numerical model and do not take into account the bulk-channel and bulk-source/drain capacitances and leakages of charge to bulk. Lumped models become inaccurate as the switching time is reduced close or below the intrinsic carrier transition time. The effects

Table 3.1: Comparison of MOSFET models for simulation of charge injection effects

Reference	Type	Channel capacitance	Partitioning	Bulk-channel capacitance	Bulk-channel leakage	Bulk-source/drain capacitance	Bulk-source/drain leakage	Tested maximum ramping rate
[21]	Numerical	Lumped	50-50 split	No	No	No	No	$5x10^8$ V/s
[22]	Numerical	Distributed	Automatic	No	No	No	No	
[23]	Numerical	Lumped	50-50 split	No	No	No	No	$5x10^8$ V/s
[24]	Numerical	Distributed	Automatic	Yes	Yes	No	No	$8x10^7$ V/s
[25]	Numerical	Two-Lumped	Automatic	No	No	No	No	$8.9x10^7$ V/s
[26]	Analytic	Lumped	50-50 split	Yes	No	Yes	No	$1x10^7$ V/s
[27]	Analytic	Lumped	50-50 split	No	No	No	No	
[28]	Analytic	Lumped	50-50 split	No	No	No	No	$3.3x10^7$ V/s
[29]	Analytic	Lumped	Manual	No	No	No	No	
[30]	Numerical	Lumped	Manual	Yes	Yes	Yes	Yes	

of the bulk-channel capacitance and the leakage from the channel to the bulk becomes significant at high switching speeds. The gate-channel capacitance in the numerical model in [22] is distributed, but the model also does not include the bulk-channel and bulk-source/drain capacitances and leakages of charge. The distributed, numerical model in [24] takes into account the bulk-channel capacitance, but the implementation of the model is difficult. The two-lumped model in [25] was proposed to overcome the inefficiency of the model in [24], but it neglected the bulk-channel capacitance and the leakage from channel to the bulk. Thus, this model becomes inaccurate when the switching time is reduced to the level of the carrier transition time. The models in [26-29] are analytical, offering simplicity in implementing the models, but these models are lumped models which are accurate only when the switching speed is slow. The numerical model in [30] has been implemented in SPICE, but this model is a lumped model, where the partitioning of the channel charge to the drain or source must be manually input. The analytical or numerical models are difficult to use if the circuit involving MOSFET switches is not trivial. In cases where the switch circuit is very simple, the accuracy of existing models is not sufficient for high performance application. An accurate macromodel, which is easily implementable in standard simulators like SPICE, offers potential for substantial improvements in modeling accuracy and offers potential for accurately simulating the switching behavior of circuits employing MOSFET switches.

The gate-channel capacitance, the cause for the channel charge injection, is geometrically distributed and not accurately modelable with a lumped transistor model. In actual circuits with MOSFET switches, the partitioning of a channel charge injected into the drain or source nodes depends on the conditions in the channel and at the nodes. These conditions are the time-varying conductance of the MOSFET switch during the turn-off transient, signal level, and the impedances at each node around the MOSFET

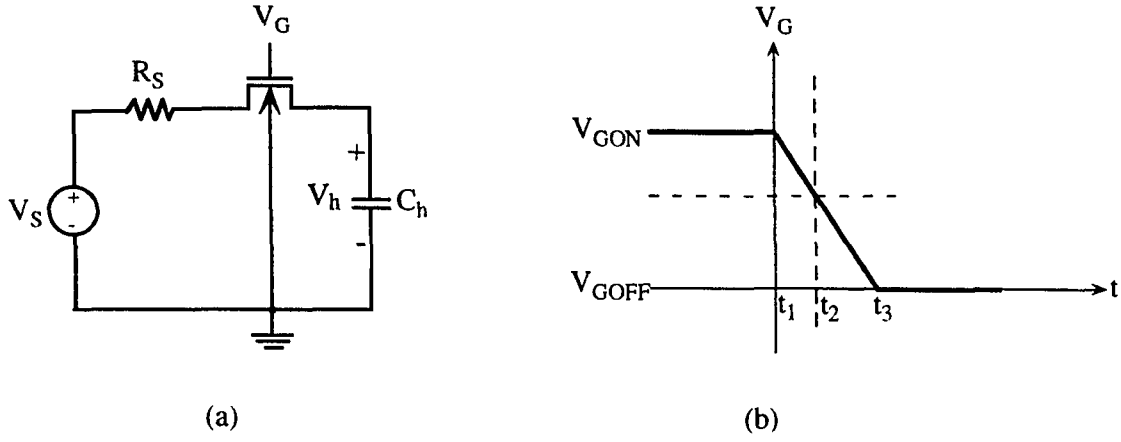
switches. When the switching speed is very fast, the effect of the time-varying capacitance between the bulk, the channel, and the leakage of the channel charge to the bulk becomes significant. The existing models, which conserve charge at the device terminals, require a manual preset input for the partitioning of the charge injected [29, 30] or divide the gate-channel capacitance and lump it at the drain and source nodes. These models are not adequate to accurately simulate the charge injection behavior of MOSFET switches and simulate the effectiveness of compensation schemes.

Thus, even though research on MOSFET switches and on compensation techniques for switch-induced disturbances in the MOSFETs is extensive, a practical model suitable for the simulation of the non-ideal behavior of circuits employing MOSFET switches has not been developed yet. The development of high-precision high-speed circuits such as sample-and-hold circuits, high resolution ADC's, and many other high precision high speed switched-capacitor or switched-current circuits demands a model that can accurately simulate the capacitive behavior as well as the conductive behavior of the switches.

In this chapter, solid state physics for MOSFETs and the disturbance induced by the MOSFET switch are reviewed using a simple sample-and-hold circuit. A charge conserving macromodel for MOSFETs is proposed. The macromodel is compared with SPICE models, including a level 2 charge conserving model. The accuracy of the macromodel is verified by experimentally measuring the clock-feed-through error voltage of a simple sample-and-hold circuit and comparing the results with the simulation results using the macromodel. The macromodel should be accurate even at higher switching speeds, because of its distributed nature, its ability to simulate the junction-like capacitance between the bulk and the channel, and its ability to simulate the leakage current into the bulk.

3.2 Qualitative Review of the Behavior of the MOSFET Switch

In this section, the mechanism which makes a MOS switch disturb the adjacent node voltages during the turn off transient period is reviewed using a simple sample-and-hold circuit. This circuit consists of an n-channel MOSFET switch and a holding capacitor as shown in Fig. 3.1 (a). As shown in Fig. 3.1 (b), the gate voltage is assumed to be a linear ramp where t_2 is the time when the MOSFET switch is at its threshold voltage. Prior to t_1, we assume the switch has been turned on for a sufficiently long time with the gate voltage of V_{GON} so the voltage across the holding capacitor has settled at V_S within a specified settling error. At t_1, charge is stored not only in the holding capacitor but also in the parasitic capacitances in the MOS switches; gate-channel, bulk-channel, bulk-source, bulk-drain junction, gate-source, and gate-drain overlap capacitances. The parasitic capacitances of n-channel MOS transistors are shown in Fig. 3.2. The distributed bulk-channel capacitance is assumed to be lumped and depicted by the capacitor C_{BC}. The



(a) (b)

Figure 3.1: (a) Sample-and-hold circuit consisting of an n-channel MOSFET switch and a holding capacitor, (b) gate voltage during turn off period

bulk-channel capacitance is a voltage-dependent junction-like capacitance.

When the voltage between the gate and the source is above the threshold, the charge in the channel, due to the gate-channel capacitance, is the accumulated minority carriers as a result of the inverted semiconductor beneath the gate oxide. The charge in the semiconductor beneath the gate oxide, due to the channel-bulk capacitance, is the ionized dopants in the semiconductor. This is a result of the depletion of the majority of the carriers in the depletion region by the influence of the gate voltage. The net charge in the channel is the charge due to the channel-bulk capacitance minus the charge due to the gate-channel capacitance. This net channel charge is negative for the n-channel and positive for the p-channel.

When the gate-source voltage is below the threshold, the channel charges due to the gate-channel capacitance and the bulk-channel capacitance cancel each other. Therefore, the net channel charge is zero in the quasi-steady state. Either below or above

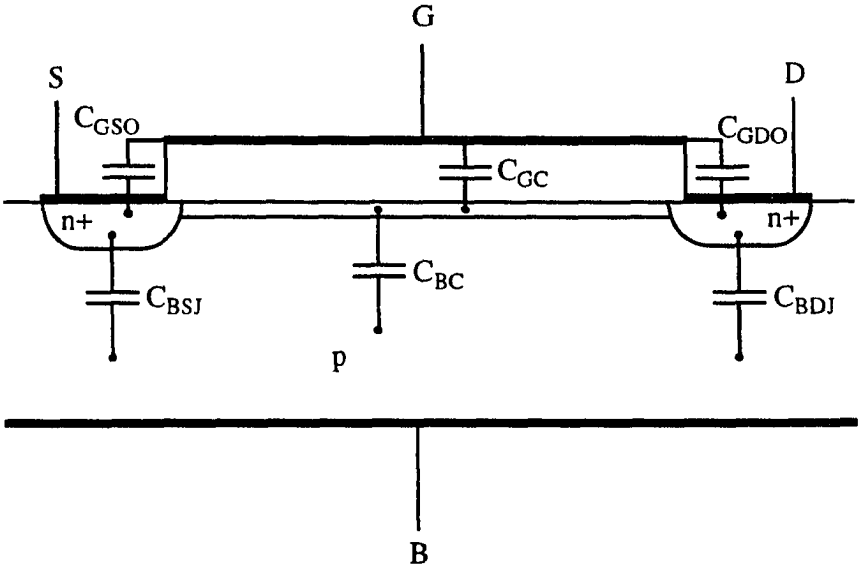


Figure 3.2: Parasitic capacitances in MOSFETs, shown for an n-channel device

threshold, the sum of the net channel charge and the charge in the depleted semiconductor should balance exactly the charge on the gate, due to the gate-channel capacitance in the quasi-steady state.

Figure 3.3 shows the energy band diagrams of an n-channel MOSFET at the threshold (a) when V_{SB}=0 and (b) when V_{SB}>0 in the quasi-steady state inside the semiconductor. The energy band diagrams exhibit the junction capacitances between the bulk and the source/drain, and the bulk-channel junction-like depletion capacitance. In Fig. 3.3, ϕ is the surface potential required for the onset of inversion and ϕ_{bi} is the built-in potential of the bulk-source/drain junction. As the gate-source voltage increases from zero toward the threshold voltage, the energy band of the substrate bends and the negatively charged depletion region (p-type substrate) widens. Note, until the gate-source voltage reaches the threshold voltage, accumulation of the minority carriers beneath the gate oxide is impossible, even though a lateral potential valley beneath the gate oxide exists. Because the potential at the valley is still higher than the potential at the source and drain for the minority carriers, the minority carriers (if any) will be spilt laterally to the drain and source. As the gate-source voltage increases over the threshold, the energy level of the valence band edge of the semiconductor beneath the gate oxide is no longer higher than that of the n+ semiconductor of the source and drain. Now, the abundant electrons in the n+ source region will flow into the region beneath the gate oxide, forming the channel, a thin layer of the accumulated minority carriers. As the gate voltage increases further over the threshold voltage, the energy band of the substrate does not bend any further, that is, it is virtually pinned at the state shown in Fig. 3.3. A little more bending will be enough to accommodate a layer of large amount of negative charge because of the high density of electron states in the valence band, since the vertical electric

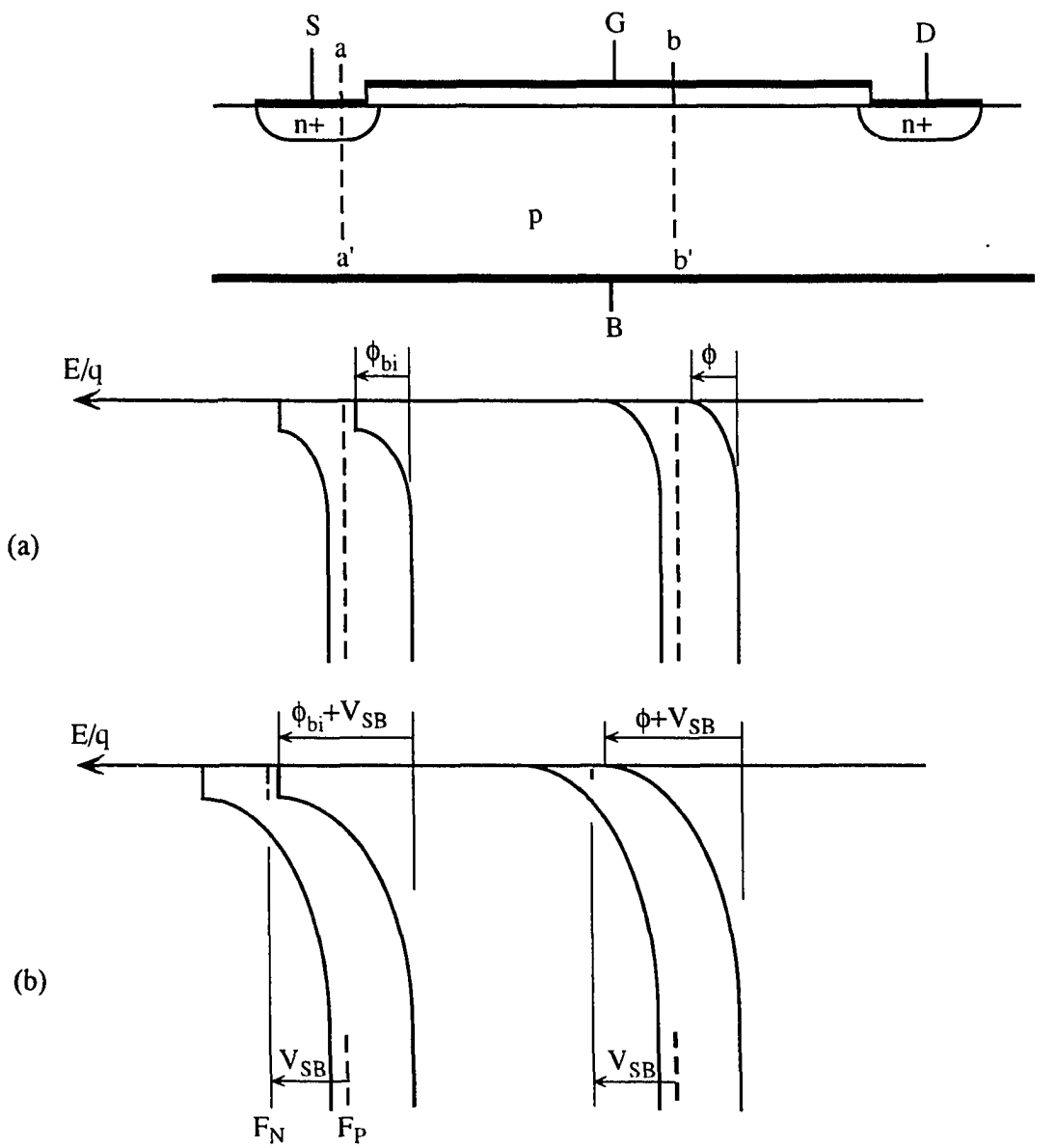


Figure 3.3: Energy band diagrams of an n-channel MOSFET inside the semiconductor along line a-a' and along line b-b'; (a) When V_{SB}=0, (b) V_{SB}>0

field across the gate oxide attracts the electrons and keeps them in the channel.

Now consider what happens when the MOSFET switch is turned off, that is, when the gate voltage falls from V_{GON} toward the threshold voltage (between t_1 and t_2). Here, the discussion is divided into two extreme cases: 1) the gate voltage falls slow enough such that as the gate voltage falls, the channel charge exits to either drain or source quickly enough to keep a quasi-steady state throughout the turn off period. And, 2) the gate voltage falls fast such that the charge in the channel cannot exit completely to either drain or source quickly enough to keep a quasi-steady state. In the latter case, the charge in the depletion region underneath the channel decreases in response to the gate-bulk voltage decrease. The depletion charge is ionized dopants and the change in the depletion charge involves movement of the majority of the carriers which is prompt. In this case, some of the channel charge leaks into the bulk during the turn off and the following transient period, because the potential barrier between the channel and the bulk is lowered. This leakage of charge into the bulk due to a fast gate voltage is called the charge pumping effect [31]. If the potential difference between the channel and bulk is reduced because of the reduced depletion region before the channel charge exits along the channel, as the gate voltage falls, some of the minority carriers in the channel leak into the bulk and recombine with the abundant majority carrier in the bulk. Because the fast surface states are passing through the Fermi level, some of the minority carriers recombine via the fast surface states. Both types of recombinations contribute to the charge pumping effect.

In the former case where the exit of the channel charge is prompt enough as compared to the speed of the gate voltage, the gate voltage falls from V_{GON} toward the threshold voltage. The minority carriers in the channel respond and quickly exit to the drain or source along the potential valley, where the depth is unchanged until the gate

voltage is decreased to the threshold voltage (the depletion region remains unchanged). Thus, between t_1 and t_2, the inside of the transistor is in a quasi-steady state. Only after the gate voltage reaches the threshold voltage, by which time the minority carrier channel charge has completely exited to the drain and source, the depletion width starts to decrease in response to the further decrease of the gate voltage. The minority carriers are not lost into the bulk because of either recombination in the bulk or in the surface states (no charge pumping effect).

In any intermediate case between the two extreme cases during the period between t_1 and t_2, the injected charge from the channel of the MOSFET switch to the holding capacitor is a source of error in the sample-and-hold circuit. In addition to this error, some of the charge on the gate-drain and gate-source overlap capacitances is also injected in response to the variation of the gate voltage, and the part of the injected charge to the holding capacitor is also a source of the error. If the disturbance in the voltage across the holding capacitor due to the injected charge during the period between t_1 and t_2 is not negligible, the voltage-dependent source-bulk and drain-bulk junction capacitances will also inject a charge in response to the variation of voltage at the drain and source. This is another source for the error of the sample-and-hold circuit. However, in a good sample-and-hold circuit and in the cases where the gate voltage is not extremely fast, the voltage along the source, channel, and drain should be constant. Thus, the effect of the injected charge from the junction capacitances should be relatively small.

Now, once V_G reaches the threshold voltage, the transistor is turned off except for a small subthreshold current. Then, the circuit shown in Fig. 3.1 (a) can be simplified as shown in Fig. 3.4, during the period between t_2 and t_3 ignoring the small leakage current. Figure 3.4, shows the gate is coupled with the drain through the gate-drain overlap capaci-

tance. As the gate voltage decreases further from the voltage at the threshold, the drain voltage as a function of the gate voltage is given by

$$V_D(t) = V_D(t_2) + \frac{C_{GDO}}{C_{GDO} + C_{BDJ} + C_h}\left(V_G(t) - V_D(t_2)\right) \quad . \tag{3.1}$$

From (3.1), it is noted that as the gate voltage decreases, the drain voltage also linearly decreases. The second term in (3.1) is another error due to the gate-drain overlap capacitance that the MOSFET switch introduces to the sample-and-hold circuit during the period between t_2 and t_3 (while the gate voltage decreases below the threshold).

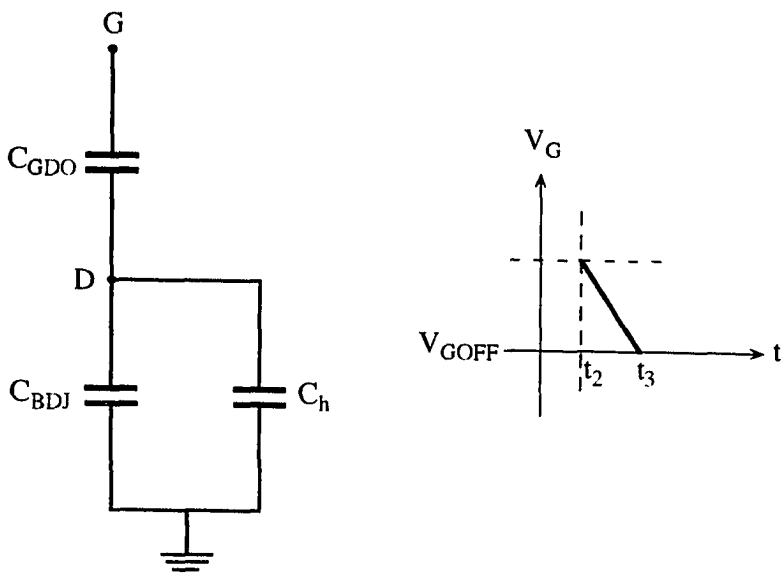


Figure 3.4: An simplified circuit of the circuit shown in Fig. 3.1 (a) during the period between t_2 and t_3

3.3 A Charge Conserving Macromodel for MOSFETs

When SPICE performs a transient analysis, the charge in the parasitic capacitances of MOSFETs is not conserved, except when the level 2 model is used with an *XQC* value less than 0.5. This is a flag to activate the charge conserving model [31]. Even when the charge conserving model is used, the partitioning of the stored charge to drain or source must be manually input. It is undecided by the time-varying conditions in the circuit, including the MOSFETs.

In SPICE, the conductance of MOSFETs is well modeled [45-47], but the capacitive characteristics of MOSFET models have the limitation mentioned above. To overcome this problem and to provide an effective means for simulating the charge injection effect of MOS switches, the macromodel shown for n-channel MOSFETs in Fig. 3.5 is proposed [39, 40] based on the nature of the parasitic capacitances in MOSFETs discussed in the previous section and utilizing the conductance models in SPICE. This macromodel can be used directly in standard circuit simulators such as SPICE.

The (n+1) MOSFETs in the circuit shown in Fig. 3.5 are used to model the channel conductance. They should be parasitic capacitance free, which is possible to implement in SPICE. All the parasitic capacitances shown in Fig. 3.2 are accounted for with external capacitors and diodes which inherently conserve a charge. If the channel dimension of the actual transistor to be modeled is WxL with lateral diffusion of L_D, the channel dimension of each of the MOSFETs, M_1, M_2,..., M_n, M_{n+1}, in the macromodel should be Wx$\{(L-2L_D)/(n+1)\}$ with zero lateral diffusion such that the series connection of

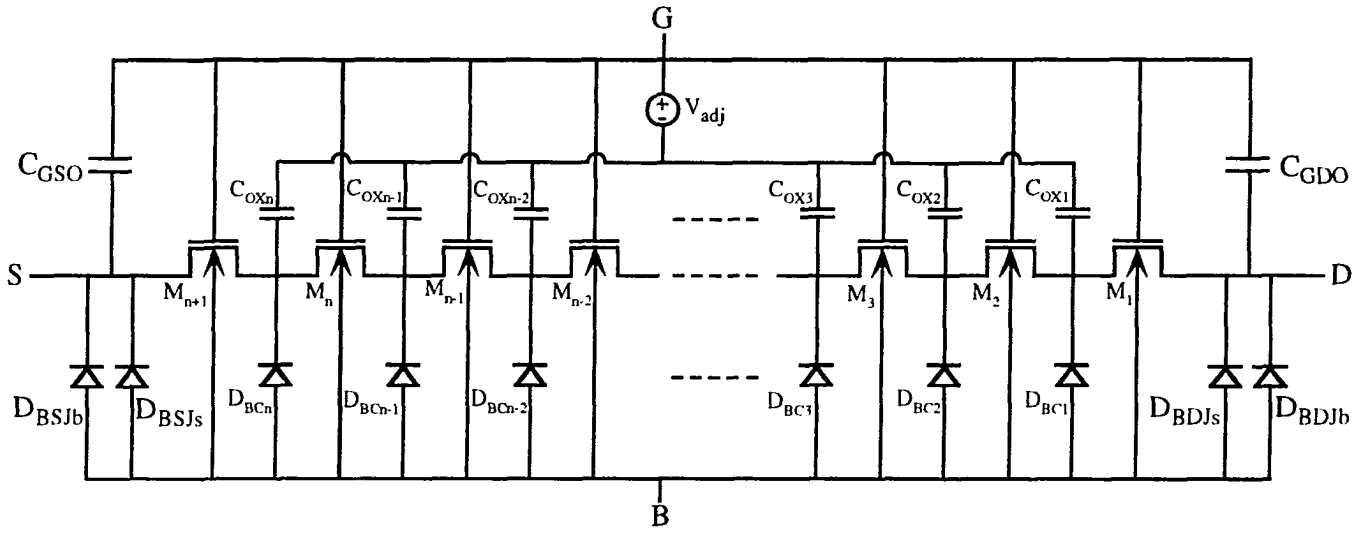


Figure 3.5: Charge conserving macromodel for MOSFETs, $V_{adj}=V_{FB}+\phi$

the (n+1) MOSFETs can model the conductance of the MOSFET of WxL with lateral diffusion of L_D. Because a MOSFET is modeled with divided MOSFETs connected in a series, the impedances seen from a point in the channel in both lateral directions by the charge at that point in the channel is appropriately accounted for in the macromodel.

The capacitors C_{GSO} and C_{GDO} model the overlap capacitances between the gate and source, and between the gate and drain, respectively.

The n capacitors, C_{OXi}, i=1,...,n, model the distributed parasitic gate-channel capacitance. The capacitance of each of the n capacitors should be the same and should be the total gate oxide capacitance of the actual MOSFET divided by n, such that the total is the same as the gate-channel capacitance of the actual MOSFET.

The diodes D_{BSJb} and D_{BSJs} model the bulk-source junction of the actual MOSFETs for both the junction capacitance and the leakage current. D_{BSJb} is the bottom junction and D_{BSJs} is the sidewall junction between the bulk and source. Similarly, D_{BDJb} and D_{BDJs} model the bottom and the sidewall junction between the bulk and drain of the actual MOSFETs.

The diodes, D_{BCi}, i=1,...,n, model the distributed depletion capacitance between the bulk and channel, and the leakage current between the channel and bulk (possible charge pumping into the bulk at high speed switching). For the total capacitance of the n D_{BCi}'s to be the same as the bulk-channel capacitance of the actual MOSFET, the dc zero bias capacitance of each n diode should be 1/n of the bulk-channel capacitance of the actual MOSFET at the onset of inversion. The diode junctions should be one-sided and abrupt with built-in potential of ϕ, which is the surface potential at the onset of inversion of the actual MOSFET. The dc zero bias junction capacitance, C_{BCiJ0}, of the D_{BCi} is related to the C_{OXi} by [48]

$$C_{BCiJ0} = \frac{\gamma}{\sqrt{\phi}} C_{OXi}. \tag{3.2}$$

When the macromodel is implemented in SPICE, the small signal zero bias junction capacitance is an input parameter for diodes half of the dc zero bias junction capacitance as given by (3.2).

To compare the MOS structure and the capacitor-diode structure shown in Fig. 3.6, first consider the voltage at the node G in the MOS structure when the voltage between node C_i and node B is V_{CBi} and the charge at node C_i is $-Q_{Ci}$. Assuming zero flat band voltage,

$$V_{GCi} = V_{Th} + \frac{Q_{Ci}}{C_{GCi}} = \phi + \gamma\sqrt{\phi + V_{CBi}} + \frac{Q_{Ci}}{C_{GCi}} \tag{3.3}$$

and

$$V_{GB} = V_{CBi} + \phi + \gamma\sqrt{\phi + V_{CBi}} + \frac{Q_{Ci}}{C_{GCi}}, \tag{3.4}$$

where C_{GCi} is the oxide capacitance of the MOS structure. On the other hand, in the capacitor-diode structure, when the voltage between node C_i and node B is V_{CBi} and the net charge at node C_i is $-Q_{Ci}$,

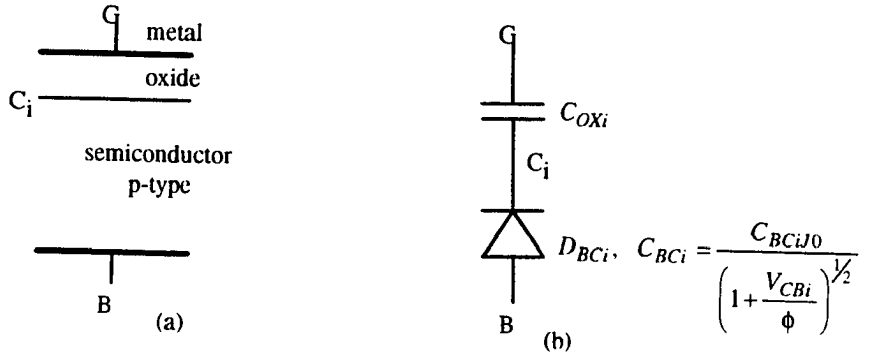


Figure 3.6: (a) MOS structure, and (b) capacitor-diode structure

$$-Q_{Ci} = -C_{OXi}V_{GCi} + (V_{CBi} + \phi)\frac{C_{BCJ0}}{\left(1 + \frac{V_{CBi}}{\phi}\right)^{\frac{1}{2}}}, \tag{3.5}$$

where the built-in potential of the diode is the same as the surface potential of the MOS structure. Using (3.2) and (3.5),

$$V_{GCi} = \gamma\sqrt{\phi + V_{CBi}} + \frac{Q_{Ci}}{C_{OXi}} \tag{3.6}$$

and

$$V_{GB} = V_{CBi} + \gamma\sqrt{\phi + V_{CBi}} + \frac{Q_{Ci}}{C_{OXi}}. \tag{3.7}$$

When C_{GCi}=C_{OXi}, from (3.4) and (3.7), we observe the voltage at node G in the capacitor diode structure is ϕ less than the voltage at node G in the MOS structure at the same charge condition and V_{CBi}.

In practical MOSFETs, at zero bias between the gate and the bulk, the energy band in the semiconductor exhibits some bending. The two main causes are the work function difference of the materials forming the gate and the bulk, and the fixed interfacial charge at the semiconductor-oxide interface. The flat band voltage, V_{FB}, is defined to be the gate-bulk voltage required to flatten the energy band in the bulk of practical MOSFETs and obtained from

$$V_{FB} = V_{T0,practical} - \phi - \gamma\sqrt{\phi}. \tag{3.8}$$

In the capacitor-diode structure, this non-ideality does not exist.

Thus, in the macromodel, the voltage at the top of the oxide capacitors should be $V_{adj} = \phi + V_{FB}$ less than the gate voltage of the MOSFETs to simulate the conductance characteristic and the capacitive characteristic simultaneously. This voltage difference is

taken care of by the voltage source of $V_{adj} = \phi + V_{FB}$ in the macromodel, assuming the fixed interface charge is constant regardless of the variation of the gate.

In this macromodel, the conductance along the channel is modeled with the SPICE MOSFET models and the distributed capacitances along the channel are modeled by the distributed capacitors and diodes along the channel. The non-linear junction capacitances and the depletion capacitance between the bulk and channel are modeled by the capacitance of junction diodes. Because of the distributed nature, the macromodel should simulate the charge injection behavior of MOSFETs, even at a very high turn off speed, and should also be able to simulate the charge pumping behavior which can be significant at a high switching speed. Because all the capacitances shown in Fig. 3.2 are effectively modeled, the macromodel should be accurate. The macromodel is easy to use because it is easily implemented in standard circuit simulators such as SPICE. A subroutine implementation of the macromodel using 5 divided capacitors to model the gate oxide capacitance (n=5) directly usable in a SPICE input file is shown in Fig. 3.7.

In the implementation, SPICE level 1 model is used for the MOSFETs in the macromodel to model the conductance of the actual MOSFET. Note that in the .model statement for the MOSFETs in the macromodel, the substrate junction saturation current, I_S, is set to zero, because the leakage current at the drain and source to the bulk is modeled by separate diodes in the macromodel. *Lambda* is set to zero because, when the macromodel is used to model a MOSFET switch, the MOSFET switch is mostly in the ohmic region. In the ohmic region, there is no physical justification to include the channel length modulation which is unnegligible and taken care of by lambda in the saturation region. If we input a value for *Lambda* to more accurately simulate the conductance of the MOSFET in the saturation region which is passed very instantly by the MOSFET switch, SPICE reduces the conductance of the MOSFET in the ohmic region to have a

```
.subckt         Macro 1  2  3  100  (ol ow)

.param p1       dl=ol/6 darea=ol/5*ow jarea=5.51e-6*ow jperi=11.2e-6+2*ow

Dbdjb   100 1                   Djb
Dbdjs   100 1                   Djs
Cgdo    1  2                    Cov
X1      1  2  4  100  202       submac (p1.dl ow)
X1      4  2  5  100  202       submac (p1.dl ow)
X1      5  2  6  100  202       submac (p1.dl ow)
X1      6  2  7  100  202       submac (p1.dl ow)
X1      7  2  8  100  202       submac (p1.dl ow)
M6      8  2  3  100             nm  l=p1.dl  w=ow
Cgso    3  2                    Cov
Dbsjs   100 3                   Djs
Dbsjb   100 3                   Djb

Vadj    2  202  dc              0.5951

        .subckt submac          1  2  3  100  202 (dl ow)
                Msub            1  2  3  100      nm  l=p1.dl  w=ow
                Coxsub          3  202            Cox
                Dbcsub          100  3            Dbc
        .ends

.model  nm  nmos                kp=p5.kpd  vto=p3.vto  gamma=p3.gamma  phi=p3.phi
+                               is=0
.model  Cov     c               2.833e-10*ow
.model  Cox     c               7.938e-4*p1.darea
.model  Djb     d               cjo=1.038e-4*p1.jarea  m=0.6604  vj=0.8  is=5.4e-15
.model  Djs     d               cjo=2.169e-10*p1.jperi  m=0.1785  vj=0.8  is=6e-16
.model  Dbc     d               cjo=0.5*p3.gamma*p3.cox/sqrt(p3.phi)*p1.darea  m=0.5
+                               vj=0.6  is=3e-16  fc=0.95

.ends

.param p2       von=5  vs=2
.param p3       kp=5.550e-5  vto=0.8120  gamma=0.2800  phi=0.6
+               ucrit=7.880e4  uexp=0.1305  esi=1.036e-10  cox=7.938e-4
.param p4       vt=p3.vto+p3.gamma*(sqrt(p2.vs+p3.phi)-sqrt(p3.phi))
.param p5       kpd=0.5*p3.kp*(1+(p3.ucrit*1e2*p3.esi/p3.cox/(p2.von-p2.vs-p4.vt))**p3.uexp)
```

Figure: 3.7 Implementation of macromodel

continuity of the conductance at the ohmic and saturation region transition. T_{QV} is also defaulted to zero to make the MOSFETs in the macromodel free of the gate oxide capacitance, because that capacitance is modeled with external capacitors in the macromodel. Similarly, all the other parasitic capacitance-related parameters for the MOSFETs in the macromodel are defaulted to make the parasitic capacitances zero.

3.4 Simulation and Comparison with SPICE Models

Simulations of the sample-and-hold circuit shown in Fig. 3.1 were completed. First, the circuit was simulated with the macromodel for the MOSFET switch and then implemented with n=10 for the division of the MOSFET and the level 1 model for MOSFETs in the macromodel. Next, simulations were done with the models in SPICE levels 1 and 2 for the MOSFET switch in the sample-and-hold circuit. The simulation results are compared in Figs. 3.8, 3.9, and 3.10. These figures show the voltage across the holding capacitor, V_h, in the sample-and-hold circuit shown in Fig. 3.1 as a function of time. In the simulation, C_h was 2pF. The initial value for the voltage V_h across the holding capacitor C_h was set to 0.5V. The signal voltage, V_S, was 2.5V (constant). The gate voltage was as shown in Fig. 3.11 and the input resistance, R_S, was 50Ω. A set of standard 1μm CMOS process parameters as shown in Table 3.2 were used. The dimension of the switch MOSFET was W=22μm and L=1.086μm such that the settling error in 20ns was less than 16μV for all cases. The diffusion area of the source and drain was assumed to be Wx2μm.

Figures 3.8 and 3.9 compare the macromodel and SPICE models in levels 1 and 2 (with XQC=.4999). Figure 3.9 is a close-up version of Fig. 3.8, showing the turn off period and the CLFT error clearly. It is clearly shown in Fig. 3.9 that the macromodel, the

Fig. 5. Comparison of the macro model with the models in SPICE level 1 and 2

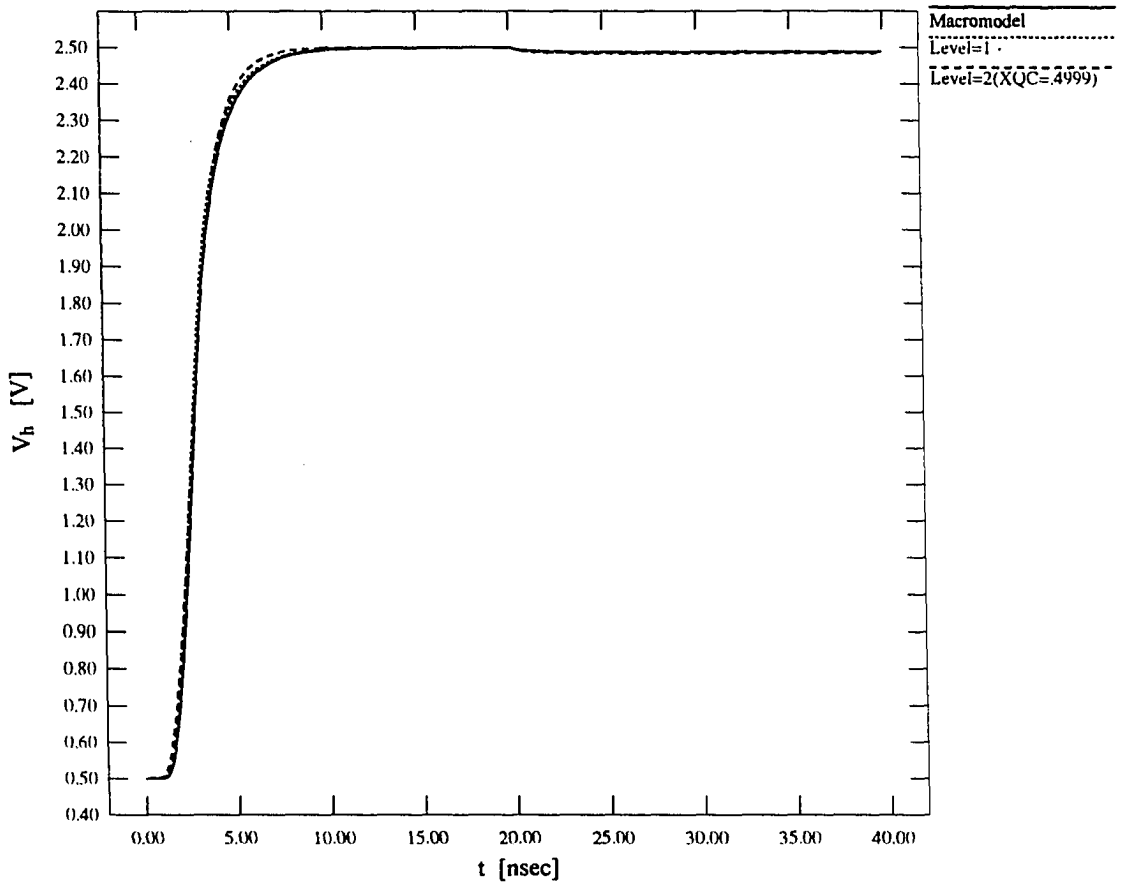


Figure 3.8: Comparison of macromodel with models in SPICE levels 1 and 2

Fig. 6. Comparison of the macro model with models in SPICE level 1 and 2

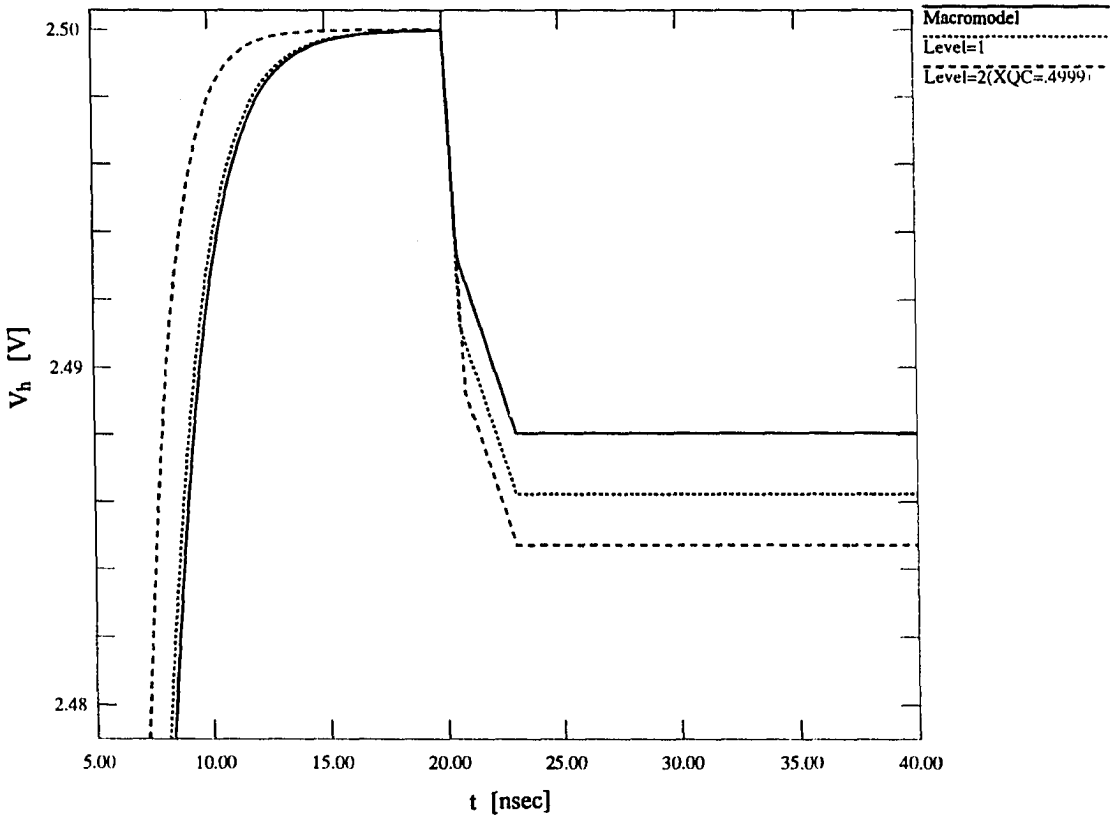


Figure 3.9: Comparison of macromodel with models in SPICE level 1 and 2

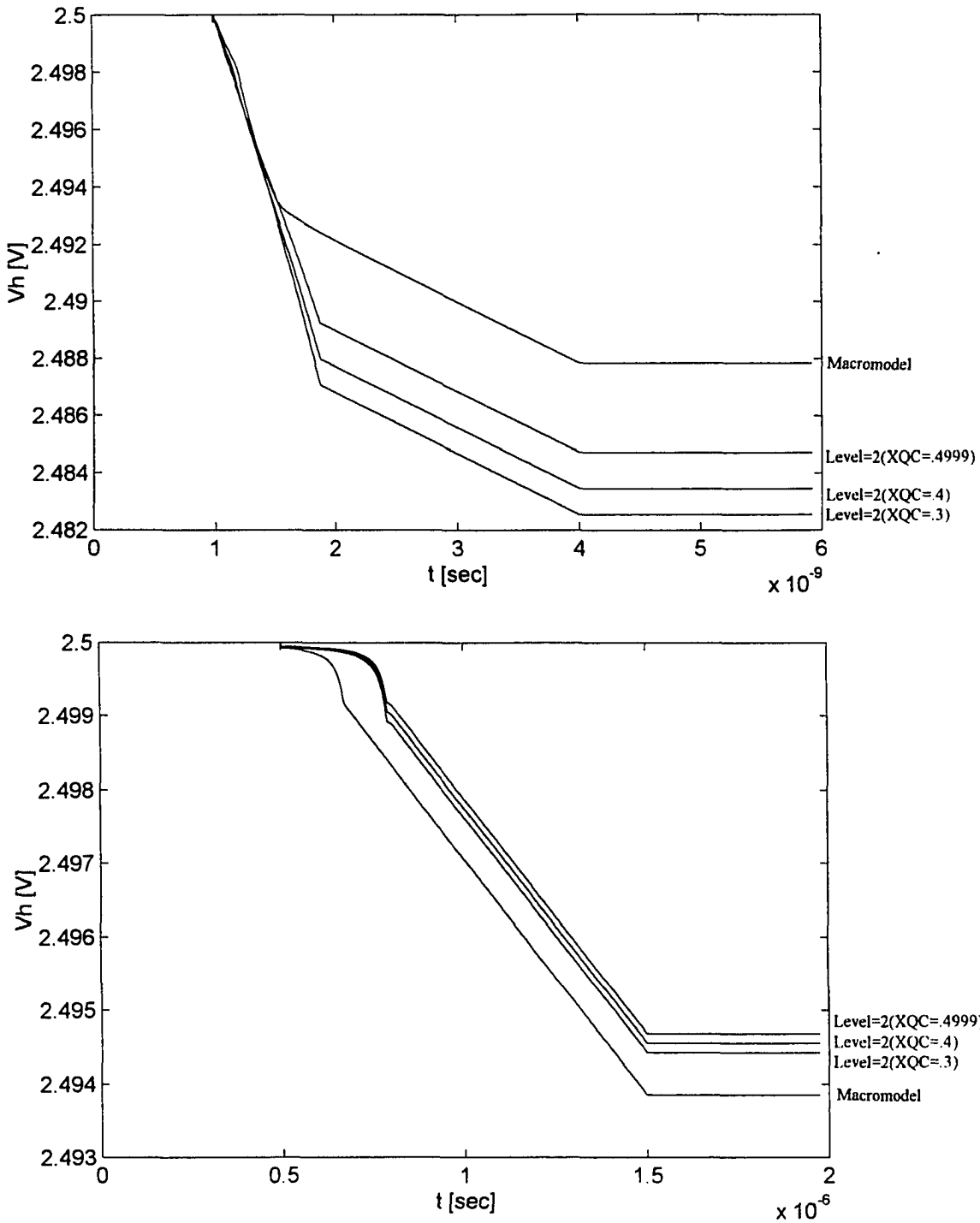


Figure 3.10: Comparison of macromodel with model in SPICE level 2.

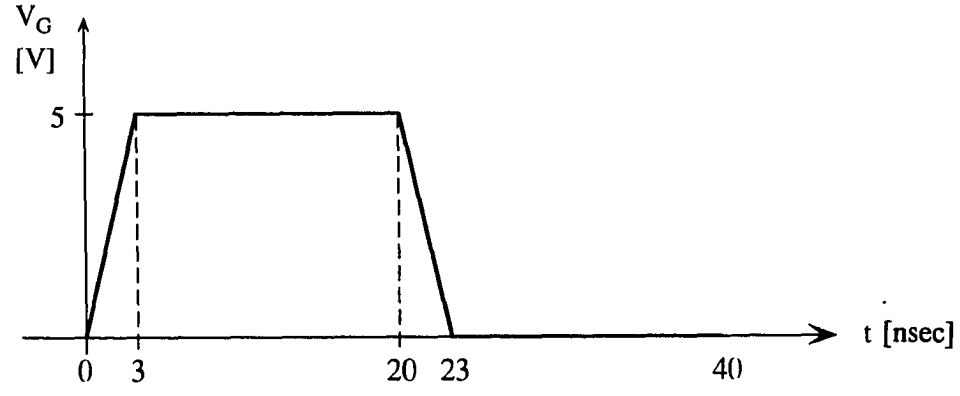


Figure 3.11: Gate voltage used in the simulation

SPICE model in level 1, and the SPICE model in level 2 (with XQC=.4999) simulate quite different CLFT error amounts as defined by

$$\text{CLFT error} = V_{h,f} - V_S \ , \tag{3.9}$$

where $V_{h,f}$ is the voltage across the holding capacitor as shown in Fig. 3.1 after the gate voltage become zero. From Fig. 3.9, the CLFT error is different by 1.81mV between the

Table 3.2: Parameter set

parameter	value	parameter	value
K'	6.432×10^{-5} A/V^2	V_{max}	9.317×10^{4} m/s
V_{TO}	0.8667 V	T_{OX}	2.502×10^{-8} m
γ	0.8088 V$^{1/2}$	C_J	2.628×10^{-4} F/m^2
ϕ	0.6833 V	MJ	0.5
$UCRIT$	1×10^{5} V/cm	C_{JSW}	3.781×10^{-10} F/m
$UEXP$	0.2728	$MJSW$	0.3
N_{sub}	8×10^{15} /cm^3	ϕ_B	0.37 V
N_{fs}	2×10^{11} /cm^2	C_{ox}	1.380×10^{-3} F/m^2
X_J	3×10^{-7} m	C_{OV}	1.173×10^{-10} F/m
μ_0	7×10^{2} cm^2/(Vxs)	C_{gbo}	3.036×10^{-8} F/m

macromodel and the SPICE level 1 model, and by 3.33mV between the macromodel and the SPICE level 2 model (with *XQC*=.4999). The voltage span is approximately 1.81mV of a least significant bit (LSB) for a 10-bit resolution, assuming the signal range is 2V. The SPICE level 1 MOSFET model is not a charge conserving model [38-40]. CLFT error simulation, using this model at different signal levels and different ramping rates for the gate voltage, showed unreasonable variation of the CLFT error.

Figure 3.10 compares the macromodel with the SPICE level 2 charge conserving model in the turn off period. In Fig. 3.10, (a) is for a ramping rate of 5V/3ns and (b) is for a ramping rate of 5V/1μs. The simulation results, using the SPICE level 2 model with *XQC* value less than or equal to 4.999, depend upon the value of *XQC*, which is a SPICE input parameter. Thus, the CLFT effect simulation utilizing the SPICE level 2 model for the MOSFET requires pre-information about the proper value for the input parameter *XQC*. The proper value for the parameter *XQC* varies, depending upon the input signal level of the sample-and-hold circuit and the gate voltage ramping rate. These facts seriously weaken the effectiveness of the charge conserving MOSFET model in SPICE level 2.

To determine the appropriate number, n, for MOSFETs, capacitors, and diodes to be used in the macromodel, simulations were done with different n's in the macromodel, keeping the other conditions constant. The results are compared in Fig. 3.12. In Fig. 3.12, a close-up version is included. When 6 MOSFETs were used (n=5), the simulation result was very close to that when 11 MOSFETs were used (n=10) down to 5V/0.1ns switching speed. However, when 2 MOSFETs were used (n=1), the simulation result showed a digression and the digression increased as the switching speed was increased to 5V/0.1ns. The intrinsic transit time is estimated to be on the order of 0.1ns, assuming a typical 1 μm process, 5V switching, and minimum MOSFET dimensions. Thus, as the

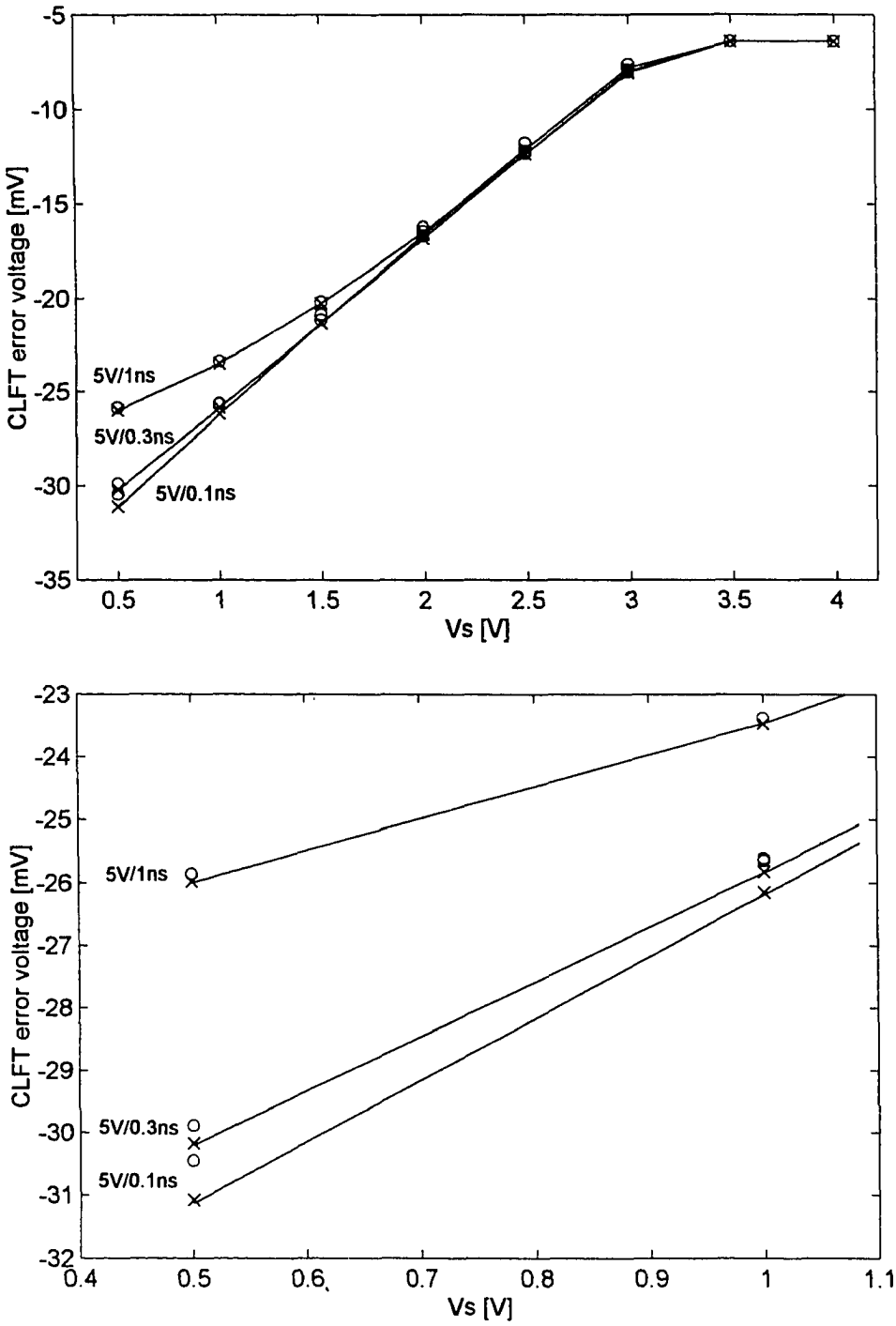


Figure 3.12: Comparison of simulation results with different numbers of MOSFETs in the macromodel: when n=10 (__), when n=5 (x), and when n=1(o)

the switching time gets close to 0.1ns, the roughly implemented (n=1) macromodel or any lumped model cannot accurately simulate the MOSFET switch.

3.5 Simulation and Comparison with Experimental Data

To verify the accuracy of the macromodel for MOSFETs, simulation results using the macromodel are compared with experimental results. Figure 3.13 shows the experimental set-up including the simple sample-and-hold circuit. The sample-and-hold circuit consisting of an n-channel MOSFET and a holding capacitor followed by a source follower was fabricated using a standard 2μm CMOS process. The micrograph of the circuit is shown in Fig. 3.14. The dimension of the MOSFET switch was W=50.40μm and L=1.490μm. The dimension of the MOSFET switch was selected such that the CLFT

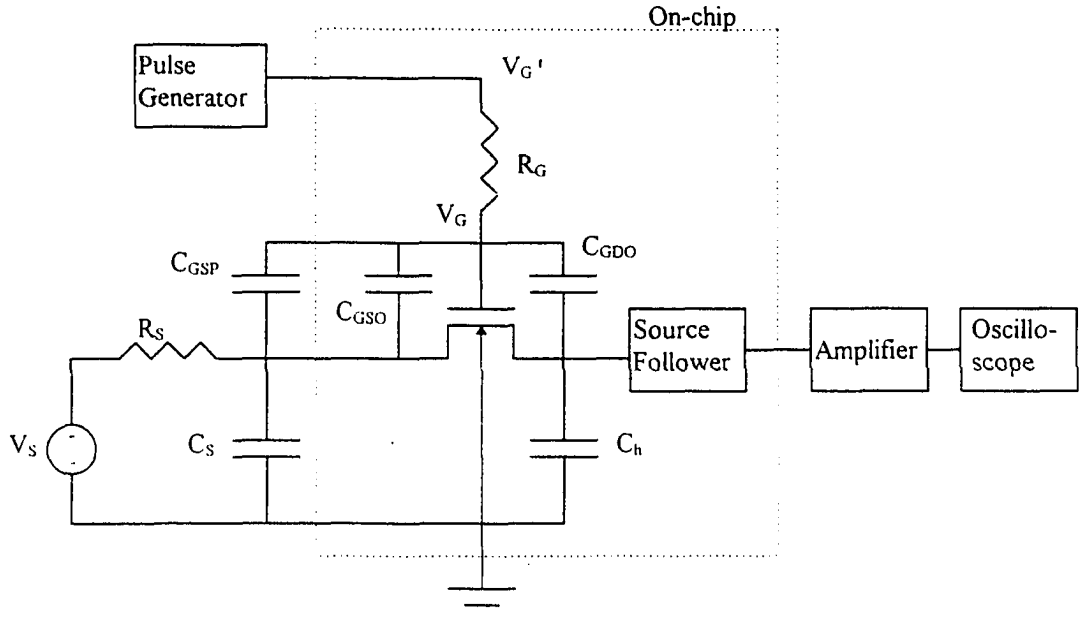


Figure 3.13: Experimental set-up

error of the sample-and-hold circuit, including the MOSFET switch, is large enough to accurately measure. In more realistic sample-and-hold circuits, the dimensions of the switch MOSFET should be carefully selected to minimize the CLFT error of the circuit meeting the settling time requirement. Table 3.3 gives the resistor values and the capacitor values for the circuit shown in Fig. 3.13. The capacitance, C_{GSP}+C_{GSO}, in Table 3.3, is the measured parasitic capacitance between the two nodes to which they are connected. C_{GSO} is the gate-source overlap capacitance of the MOSFET and C_{GSP} is the additional parasitic capacitance existing between the nodes in the actual experimental set-up. The capacitor, C_S, was externally connected to suppress the effect of C_{GSP} and C_{GSO}. Without C_S, the large C_{GSP}+C_{GSO} pushes down the voltage at the source node as the gate voltage rapidly decreases in the turn off period. In this case, it is difficult to simulate the CLFT effect. Lead inductances also prevent problems for experimental evalution. A typical lead inductance is in the range of 1nH. C_S also suppresses the effect of the parasitic inductance existing between the signal source and the source node. To test the effect of the parasitic inductance on the CLFT error, SPICE simulation was done with inductance of up to 10nH inserted between R_S and the source of the MOSFET in Fig. 3.13. When C_S is included, the effect of the parasitic inductance of up to 10nH was negligible. R_G was included in the design to suppress the effect of the parasitic inductance between the pulse generator and the gate of the MOSFET. This was also tested with a simulation. The simulation showed that R_G effectively eliminated the impact of the lead inductance in the gate. The circuit diagram of the source follower in Fig. 3.14 is shown in Fig. 3.15. The designed dimensions of the MOSFETs in the source follower are also shown in the circuit diagram. The substrate of each MOSFET is connected to its source in the source follower.

The SPICE Level 1 model was used for the MOSFETs in the macromodel because

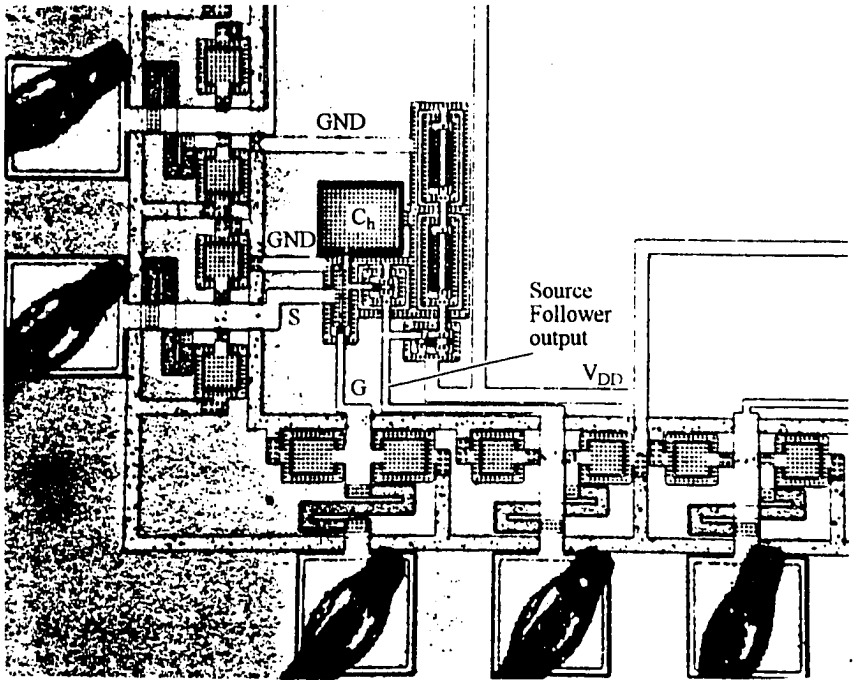


Figure 3.14: Micrograph of the sample-and-hold circuit

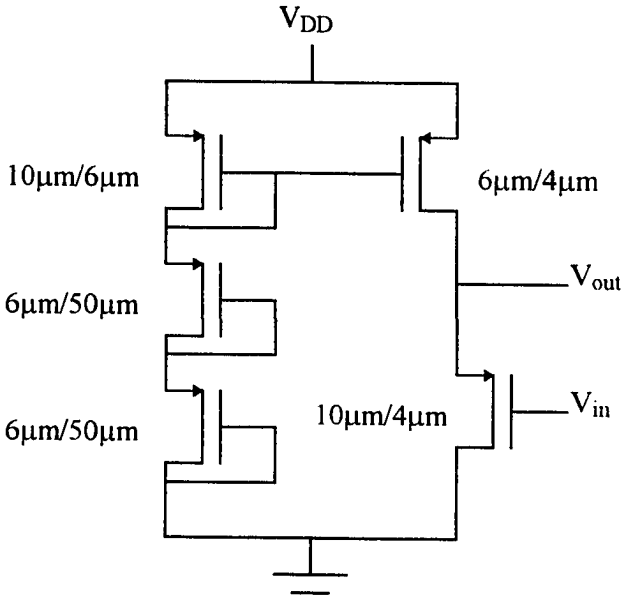


Figure 3.15: Circuit diagram of source follower

Table 3.3: Circuit parameters

parameter	value	parameter	value
R_S	50 Ω	C_h	1.937 pF
R_G	425 Ω	C_S	1 nF
		$C_{GSP}+C_{GSO}$	9.3 pF

the principles used in the development of the macromodel are consistent with the MOSFET model in SPICE level 1. The SPICE input parameters used in the simulation are given in Table 3.4. The parameter values in Table 3.4 are the extracted values using the heuristic algorithm discussed later in section 3.6. For the division of the MOSFET in the macromodel, n=10 was used. The diffusion areas of the source and drain were Wx(5μm+2L_D) in the simulation. The mobility degradation was incorporated in the simulation with the macromodel utilizing the .PARAM statement in SPICE, as shown in Fig. 3.7. The mobility degradation incorporated in the simulation modifies K', depending on V_S [20], [45] by

$$K'_{modified} = \frac{1}{2}K'\left\{1+\left[\frac{UCRIT\varepsilon_{si}}{C_{OX}(V_{GON}-V_S-V_{TH})}\right]^{UEXP}\right\}, \tag{3.10}$$

where

Table 3.4: Parameter set

parameter	value	parameter	value
K'	5.550x10^{-5} A/V^2	C_J	1.038x10^{-4} F/m^2
V_{TO}	0.8120 V	MJ	0.6604
γ	0.2800 V$^{1/2}$	C_{JSW}	2.169x10^{-10} F/m
ϕ	0.6 V	$MJSW$	0.1785
$UCRIT$	7.880x10^4 V/cm	ϕ_B	0.8 V
$UEXP$	0.1305	C_{ox}	7.938x10^{-4} F/m^2
		C_{gdo}	2.833x10^{-10} F/m

$$V_{TH} = V_{TO} + \gamma\left(\sqrt{\phi + V_S} - \sqrt{\phi}\right) \quad . \tag{3.11}$$

Figure 3.16 (a)-(e) shows the observed ramp voltages of five different ramping rates at the node V_G' in Fig. 3.13 used in the experiments. The five ramp voltages in Fig. 3.16 were modeled with piece-wise-linear model in SPICE and shown in Fig. 3.17. Figure 3.17 (a)-(e) are the piece-wise-linear models for Fig. 3.16 (a)-(e), respectively. The modeled waveforms of V_G' and the simulated voltages at the gate, V_G, are shown together in Fig. 3.17. Once the MOSFET switch is turned off, the waveform below the threshold voltage does not affect the CLFT error. Thus, the piece-wise-linear voltage does not have to be accurate, while the gate voltage, shown together in Fig. 3.17, is below threshold as long as it decreases exactly to zero.

The CLFT error voltage of the experiment measured given by (3.9) is induced by the MOSFET switch during the turn off period of the sample-and-hold circuit. The measured CLFT errors, as a function of the signal level for the five different ramp voltages, are compared with the simulated error using the macromodel in Fig. 3.18. In Fig. 3.18, the simulation and experimental results for the five different ramp voltage are distinguished by the labels (a)-(e). The data labeled (a) are for the ramp voltage labeled (a) in Fig. 3.16 and 3.17, and so forth. The simulated CLFT error agrees with the experimental CLFT error with a maximum difference of 1.31mV, when V_S is 0.5V and the ramp waveform is (e) in Fig. 3.16. This demonstrates the capability of the macromodel of simulating the CLFT effect of the MOSFETs. When the ramp voltages observed are approximated with linear ramp voltages in the simulation with the linear ramping rates of 5V/1μsec for the observed voltage shown in Fig. 14 (a), 5V/100nsec for (b), 5V/20nsec for (c), 5v/10nsec for (d) and 5V/5nsec for (e), the simulated CLFT error

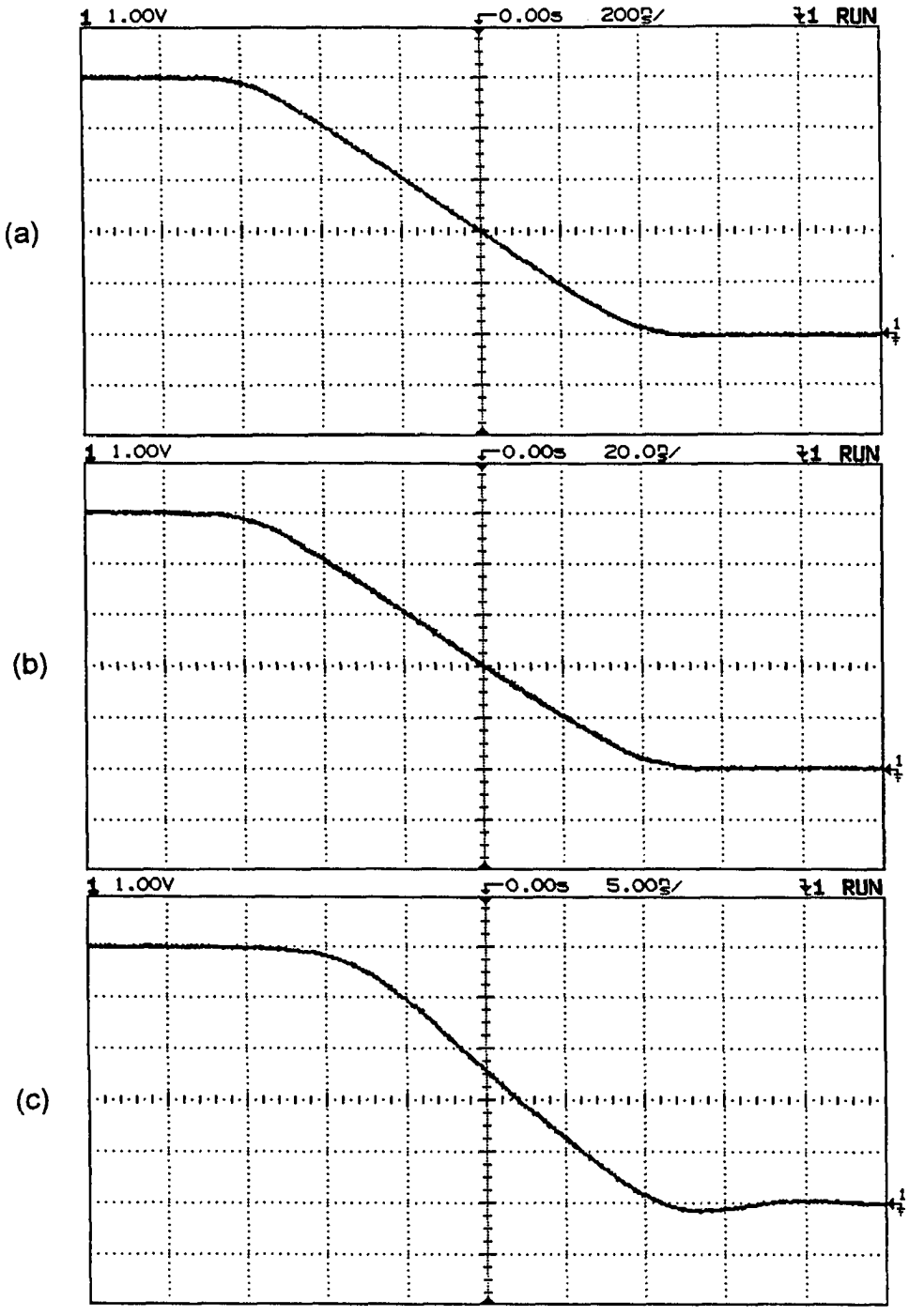
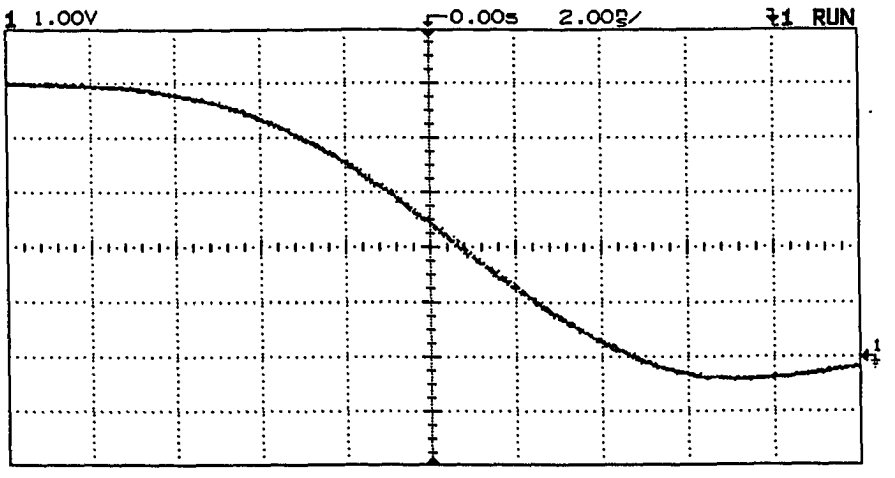


Figure 3.16: Observed ramp voltages used in the experiment

(d)



(e)

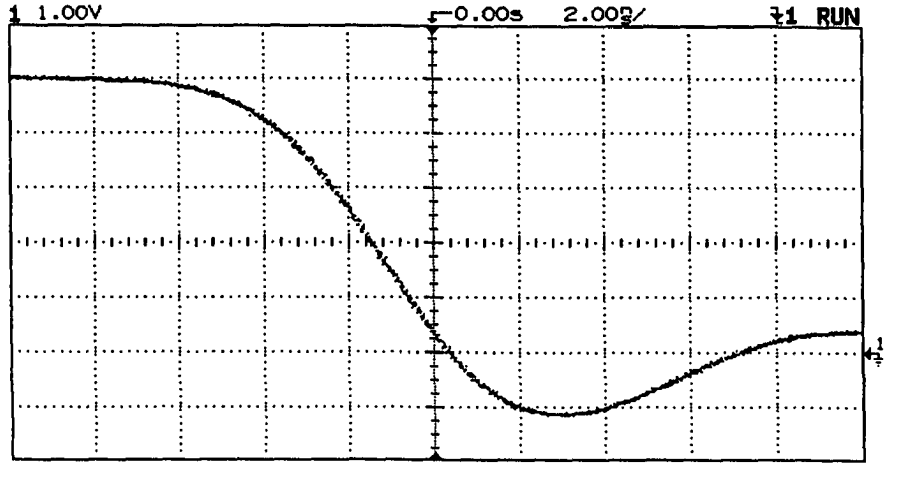


Figure 3.16: (Continued)

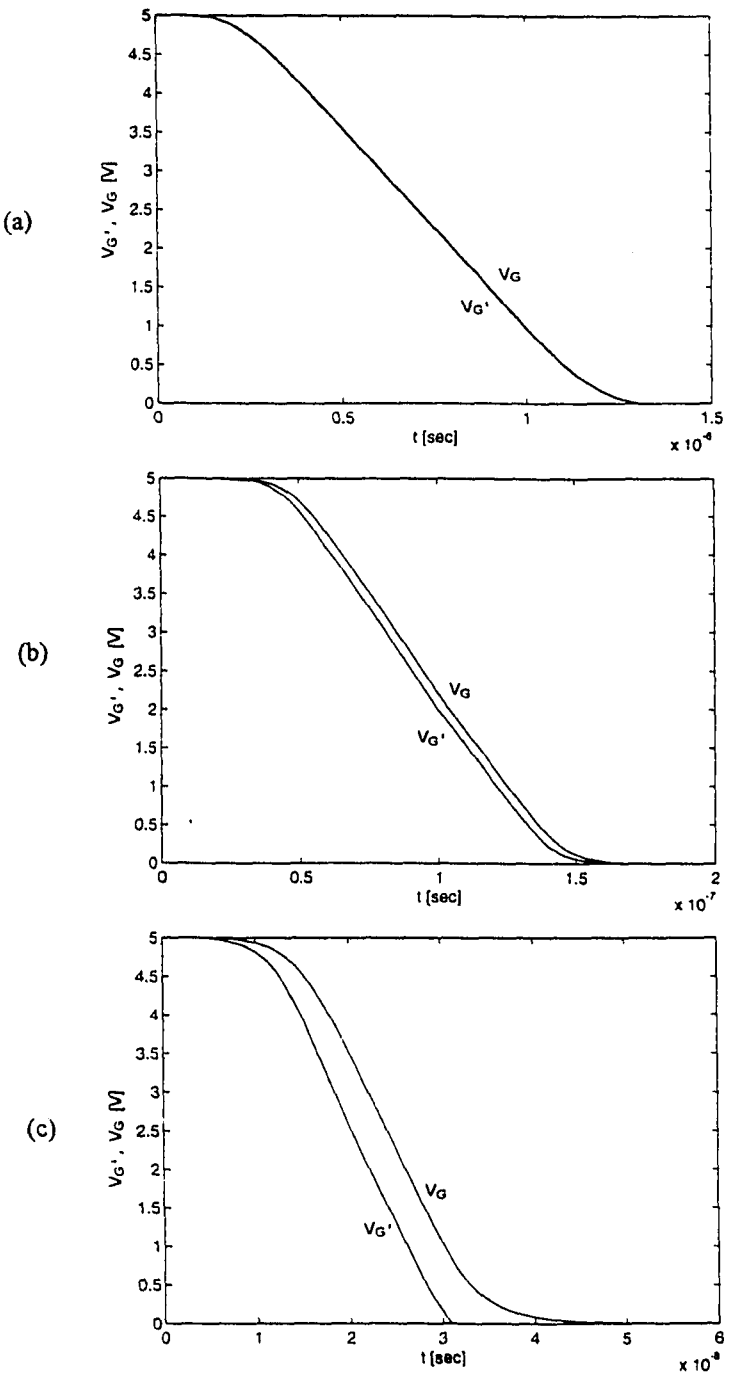
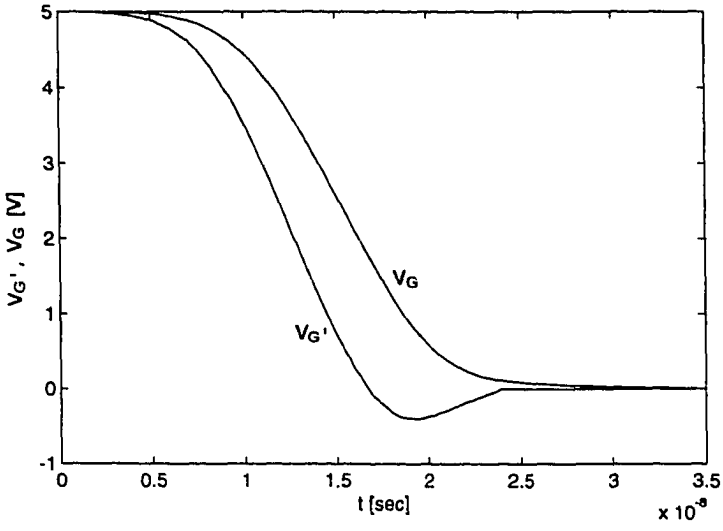


Figure 3.17: Piece-wise-linear ramp used in the simulation and the simulated gate voltage

(d)



(e)

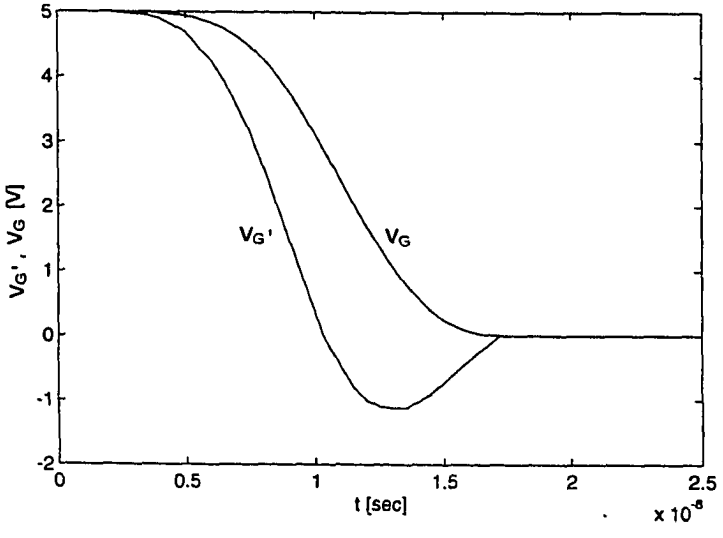


Figure 3.17: (Continued)

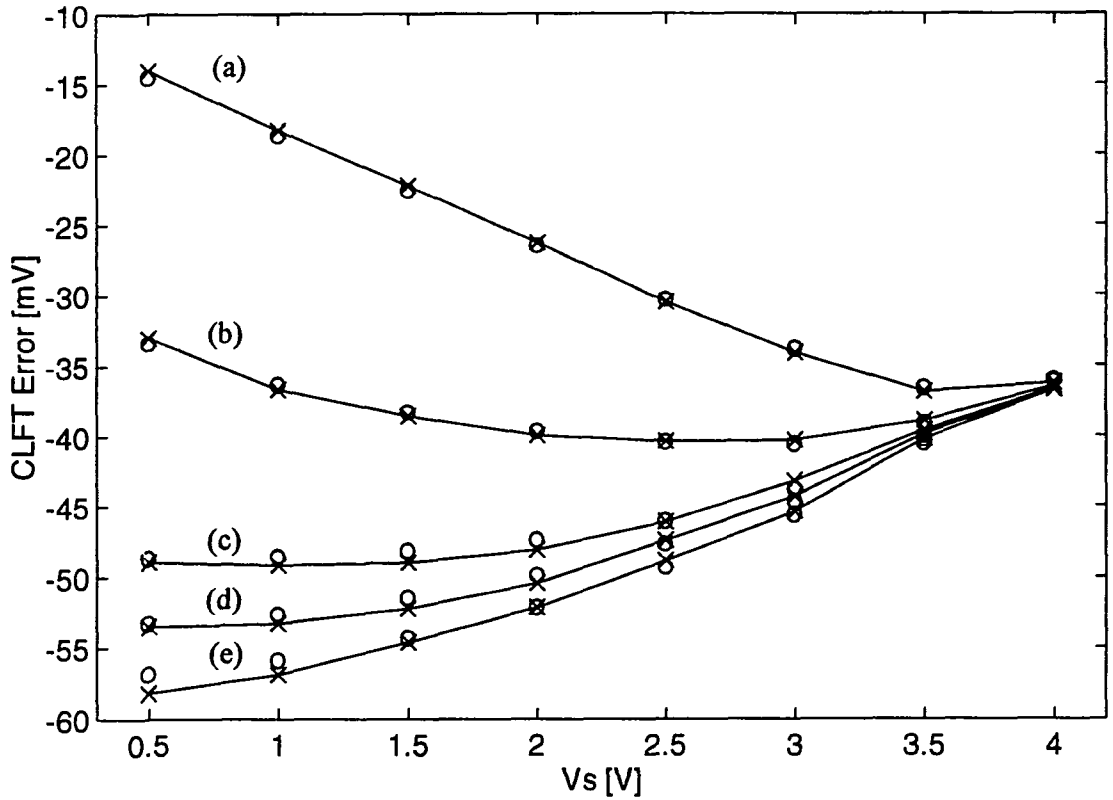


Figure 3.18: Comparison of CLFT error simulated using macromodel (o) with experimental data (-x-) when piece-wise-linear ramp is used in simulation

voltages using the macromodel are as compared with the experimental CLFT error voltage in Fig. 3.19.

These comparisons show that the implementation of the macromodel with a relatively simple SPICE level 1 model is quite accurate. When a MOSFET is used as a switch, the MOSFET is mostly in the ohmic region or in the cutoff region. Thus, many of the features of the complicated higher level models, which usually take longer simulation time and sometimes experiences convergence problems, are unnecessary, except the surface mobility degradation which is not negligible even in the ohmic region. The mobility degradation has been incorporated in the macromodel implemented with the SPICE level 1 model as explained earlier in this section.

3.6 Heuristic Algorithm for Extraction of Process Parameters

When a chip is fabricated, the lot average parameter values and/or parameter values extracted from a selected wafer are usually given. However, the exact parameter values for the specific chip are not usually given. To compare the experimentally measured CLFT errors with the simulation results using the macromodel implemented in SPICE using the level 1 model for the MOSFETs in the macromodel, the following heuristic algorithm was used to extract the values for the necessary parameters for the simulation with a macromodel from the given lot average parameter values and the extracted parameter values for SPICE level 2 MOSFET model for a selected wafer.

Initially, values for the necessary parameters are set as follows:

1. Extract C_h from the designed dimensions of the capacitor and the lot average value for the capacitance density between the layers forming the capacitor.
2. Set $W=W_{drawn}-DW$ and $L=L_{drawn}-L_D$ using the lot average values of DW and L_D.

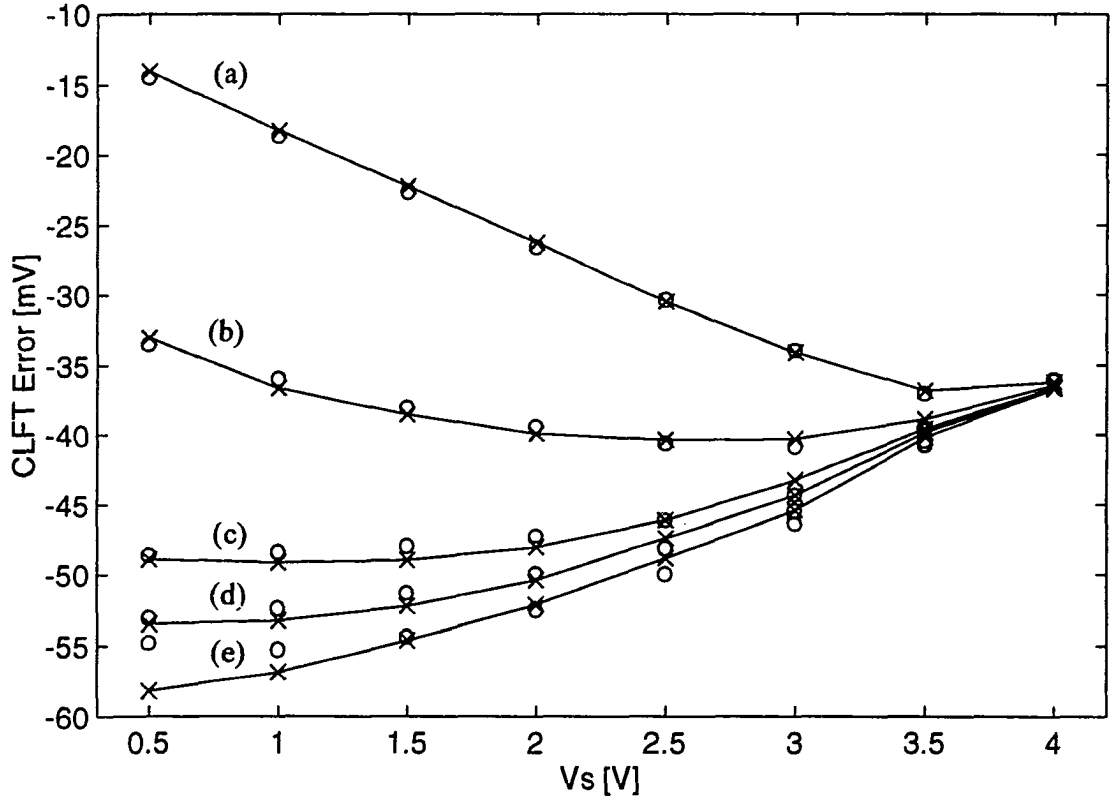


Figure 3.19: Comparison of CLFT error simulated using macromodel (o) with experimental data (-x-) when linear ramp is used in simulation

3. Set C_{gdo} using the extracted value for a selected wafer.
4. Set C_{OX} from $C_{OX}=\varepsilon_{OX}/T_{OX}$ using the lot average value for T_{OX}.
5. Set γ using the lot average value.
6. Set K', *UCRIT*, *UEXP* and V_{TO} using the extracted values for a selected wafer.
7. Set *Lambda*=0 and set the other parameters using the extracted values for a selected wafer or using the required suitable values for the macromodel.

Now, simulate the CLFT errors of the sample-and-hold circuit as shown in Fig. 3.13 with the macromodel for the MOSFET for the five ramp waveforms in Fig. 3.17 and for eight V_S values equally intervalled from 0.5 to 4V. Comparing the experimental and simulation CLFT errors, adjust the parameters to have the best match between the experimental and simulation CLFT errors using following steps;

8. Adjust C_{gdo} for the best match of the experimental and simulation CLFT error at the highest V_S (4V).
9. Adjust either K' or *UCRIT* such that the cost function defined by

$$\max_{i,j}\left(\left|\frac{X_{mij}-X_{sij}}{X_{mij}}\right|\right) \tag{3.12}$$

is minimized where X is the CLFT error, subscript m represents measured, subscript s represents simulated, subscript i represents eight different V_S equally intervaled from 0.5 to 4V, and subscript j represents the five different ramp waveforms. The adjustment of K' and the adjustment of *UCRIT* can have same effect on the simulated CLFT error as suggested by (3.10). From (3.10), it is seen that increasing the value of either K' or *UCRIT* increases $K'_{modified}$. In the extraction to obtain the parameter values in Table 3.3, when K' was increased by a factor of x, *UCRIT* was also increased by a factor of $(1.09x)$.

10. Adjust W and L such that the cost function given by (3.12) is minimized.
11. Adjust V_{TO} such that the cost function given by (3.12) is minimized.
12. Adjust γ such that the cost function given by (3.12) is minimized.
13. Adjust $UEXP$ such the cost function given by (3.12) that is minimized.

If necessary, repeat steps 9 to 13.

The parameter values in Table 3.4 have been extracted using this heuristic algorithm. Table 3.5 compares the extracted parameter values using this heuristic algorithm with the initial values and also shows the average values of 13 runs of the same process. When the initial parameter values are used in the simulation of the CLFT error using the macromodel, the simulation results are as compared with the experimental CLFT error as shown in Fig. 3.20. The maximum difference between the simulated and experimental CLFT errors is 2.48mV, while it is 1.31mV when the extracted parameter values using the heuristic algorithm is used in the simulation.

Table 3.5: Comparison of process parameters

parameter	average	initial value	final value
C_{gdo}	3.410×10^{-10} F/m	2.852×10^{-10} F/m	2.833×10^{-10} F/m
K'	4.781×10^{-5} A/V^2	4.549×10^{-5} A/V^2	5.550×10^{-5} A/V^2
$UCRIT$	7.836×10^{4} V/cm	5.916×10^{4} V/cm	7.880×10^{4} V/cm
W	50.34 μm	50.40 μm	50.40 μm
L	1.552 μm	1.520 μm	1.490 μm
V_{TO}	0.8372 V	0.8756 V	0.8120 V
γ	0.2100 V$^{1/2}$	0.2200 V$^{1/2}$	0.2800 V$^{1/2}$
$UEXP$	0.1555	0.1592	0.1305

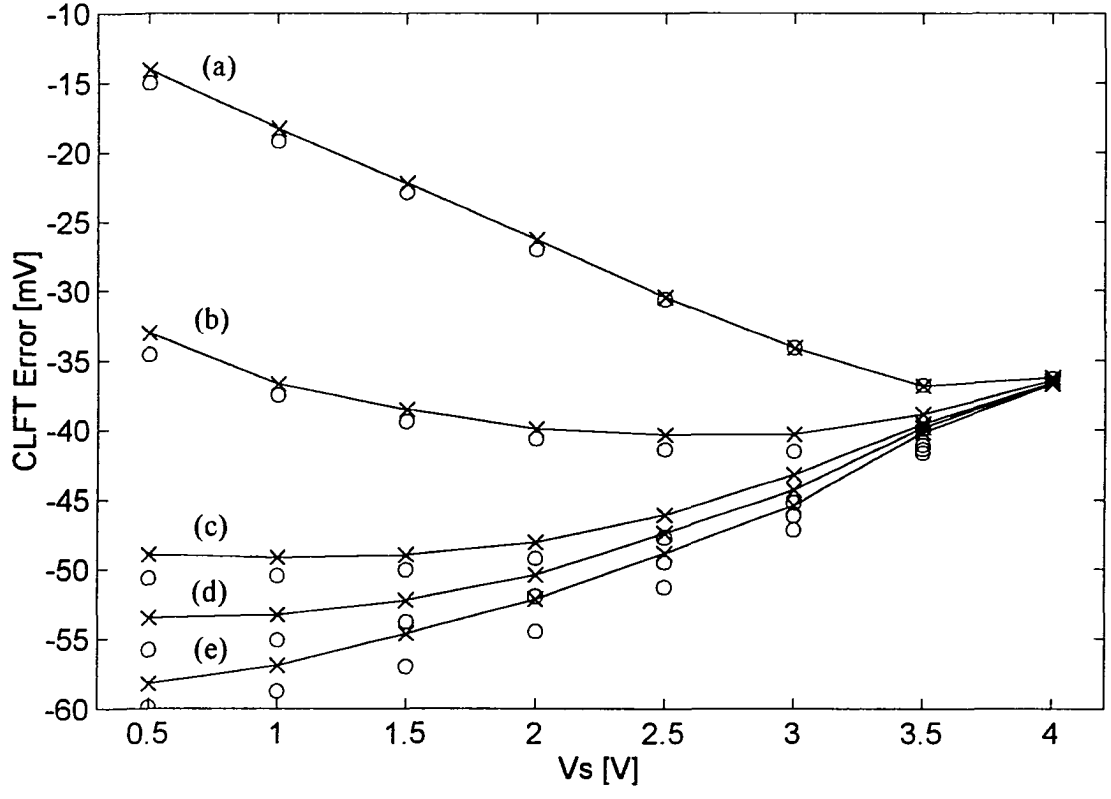


Figure 3.20: Comparison of CLFT error simulated using macromodel (o) with experimental data (-x-) when initial parameter values and piece-wise-linear ramps are used in simulation

3.7 Conclusions

The mechanism which makes a MOSFET switch inject charge to the adjacent node and disturb the node voltages during the turn off transient period has been reviewed. Based on this review, a charge-conserving macromodel for MOSFETs useful for simulating the charge injection effect of MOSFET switches has been presented. All the capacitances involved in a MOSFET are taken care of with the external charge conserving capacitors and diodes in the macromodel. The diodes in the macromodel will also take care of the leakage currents which become significant at a high switching speed. The implementation of the macromodel for a MOSFET, assuming SPICE as the simulator, has been discussed in detail showing a .subckt example implementation. This macromodel can be used directly in standard circuit simulators such as SPICE. To show the validity of the macromodel and the problems with the SPICE models for MOSFETs, simulations were run and the macromodel was compared with SPICE MOSFET models. Finally, to test the accuracy of the macromodel, experiments were completed and compared with the simulation results using the macromodel. The difference between the experimental and the macromodel simulated CLFT error of a simple sample-and-hold circuit was a maximum of 1.31mV, where the experimental CLFT error was 58.18mV. In the macromodel, the distributed parasitic capacitances along the channel are modeled with divided external capacitors and diodes. The leakage currents to the bulk are modeled with the diodes leakage currents. The channel conductances can be well modeled with the MOSFET models in simulators like SPICE. Because of this nature, the macromodel should simulate the charge injection behavior of MOSFETs accurately, even at a very high switching speed.

It is believed that when we can accurately simulate the charge injecting behavior of the MOSFET switches, we can effectively attempt to solve the problem which has hindered the analog and mixed signal circuit design. A charge conserving macromodel for MOSFETs has been developed in an effort to provide an accurate and effective means for the simulation and understanding of the non ideal phenomenon of the charge injection of MOSFETs.

The maximum difference between the experimental and the simulated CLFT error using the macromodel was 1.31mV, when the extracted process parameters by the heuristic algorithm were used. With the parameters obtained from the lot average and from a test circuit on a selected wafer of the run, the maximum difference between the experimental and the simulated CLFT error using the macromodel was 2.48mV. These differences will be scaled down, if the ratio of the dimension of the MOSFET switch to the dimension of the holding capacitor is reduced in realistic cases. Furthermore, in a compensated sample-and-hold circuit, it is believed that the difference will be reduced proportional to the decrease of the magnitude of the CLFT error of the compensated sample-and-hold circuit. On the other hand, the simulated CLFT error using the SPICE level 2 charge conserving model showed a maximum difference of 5.30mV from the simulated CLFT error using the macromodel in the case where the overall magnitude of the CLFT error was less by approximately a factor of 5. Thus, it is believed that the macromodel will improve the simulation accuracy approximately 10 to 20 times, 20 times when the accurate process parameters for the transient analysis of the sample-and-hold circuit, in which the MOSFET switch transits mostly between the ohmic and cutoff regions are available. This simulation accuracy improvement corresponds to a 3 to 4 bit more resolution in designs of sample-and-hold circuits and any such circuits employing MOSFET switches.

Advances in circuit design technology pursue faster and more precise circuits. Thus, the design of the circuits involving MOSFET switches has been more exacting. Even though many techniques to compensate the non-ideal charge injection effect of the MOSFETs have been developed, it was quite difficult to accurately understand the behavior of the MOSFETs or to test the effectiveness of the compensation schemes. It is believed that the macromodel should be helpful in solving problems involving the charge injection effect of the switches. The macromodel can conveniently and accurately simulate the effectiveness of the compensation schemes and can be used for the further development.

CHAPTER 4. CONCLUSIONS

In this dissertation, separate topics were presented in Chapters 2 and 3. Both topics support the high performance analog and mixed signal integrated circuit design field.

In Chapter 2, versatile finite gain amplifiers especially suitable for monolithic applications were presented. The versatile finite gain amplifiers were realized by employing active voltage attenuators consisting of MOSFETs in the feedback path of operational amplifiers. The attenuators included two different types of single input attenuators and a summing attenuator that was derived from one of the single attenuators. The summing attenuator is expandable to multiple inputs. The amplifiers realizable with the attenuators and an operation amplifier are two different kinds of single input finite gain amplifiers, a summing amplifier, and a differential or subtracting amplifier. By combining the amplifiers, it is possible to construct multiple input summing and subtracting amplifiers. The attenuators and amplifiers were analyzed for dc transfer characteristics, harmonic and intermodulation distortion, output noise voltage, and frequency response. Design methods for realizing attenuators for minimum noise and for minimum power consumption were discussed and simulation results were presented. The actual performance of the attenuators and amplifiers were characterized with experiments on specially fabricated monolithic amplifiers and attenuators. In the experiments, the linearity and the range of the linear region of the attenuator and amplifiers were first characterized

by measuring the dc transfer characteristics. Then, the accuracy of the attenuators and amplifier gains were determined by comparing the measured gains with the simulated gains using the models developed. Finally, the degree of linearity as a function of the input or output voltage range was characterized by measuring the harmonic and intermodulation distortion as a function of the input or output amplitude.

The active attenuators have several attractive characteristics. These merits include small size, nearly infinite input impedance, low power consumption, and offset adjustability independent of the attenuation ratio. It is verified experimentally that amplifiers can be built with gains that are accurate to the design value with 0.5-2% error. A single input amplifier exhibited a maximum signal output to total non-signal output ratio of 58.9dB at an output amplitude of 129mV(0-P), a summing amplifier exhibited the ratio of 55.0dB at 98.6mV, and a differential amplifier exhibited the ratio of 66.2 dB at 482mV. It is believed that the attenuators and the finite gain amplifiers realized with the attenuators should find applications in integrated analog and mixed-signal systems.

In Chapter 3, non-ideal effects induced by the MOSFET switch were discussed. A charge conserving macromodel for MOSFETs was developed in an effort to provide an accurate and convenient means for the simulation and understanding of the non-ideal phenomenon of charge injection of MOSFET switches. The macromodel was formed by taking into account the nature of the capacitances and leakage currents to the bulk in MOSFETs. The macromodel was compared with the MOSFET models in SPICE which are known to have problems with accurately predicting the charge injection effects inherent when rapidly switching the MOSFET. The accuracy of the charge conserving macromodel for MOSFETs was tested by measuring the performance of a simple sample-and-hold circuit and comparing the measurements with simulation results obtained by using the macromodel. The simulated error voltages of a simple sample-and-hold circuit

using the macromodel over wide ranges of input voltage and switching speed agreed with the experimental results to within 1.31mV. It is conjectured that the macromodel can improve the simulation accuracy of sample-and-hold circuits beyond that attainable with the SPICE level 2 charge conserving model by a factor of 10 to 20. This conjectured simulation accuracy improvement corresponds to 3 to 4 bits more resolutions in the design of sample-and-hold circuits and other circuits employing MOSFET switches.

In the macromodel, the parasitic distributed gate-channel and bulk-channel capacitances are modeled with a large number of lumped capacitors, the charge pumping to the substrate (problematic when the transition of the gate voltage is fast) is modeled by the leakage current of diodes, and the conductance in the channel is modeled with a large number of series-connected MOSFETs. These features make the macromodel effective for the accurate simulation of the charge injection of MOSFET switches.

Existing simulators depend upon lumped models of the MOSFET. When the switching speed of the MOSFET switch is fast, the lumped models fail. Existing analytic or numerical models are difficult to use if the circuit including the MOSFET switches is not simple. Thus, it is believed that the macromodel should be useful for helping designers minimize the problems associated with charge injection of MOSFET switches as the advances in technology require faster and more accurate switched circuits. Of particular interest should be the use of the macromodel in the design circuits that are intended to compensate for clock-feed-through and/or charge injection in sample-and-hold circuits.

In this dissertation, two topics were investigated that addresses two inherent problems associated with monolithic analog and mixed-signal design. These focused on the practical design of finite gain amplifiers and on developing a macromodel effective for the simulation of charge injection effects of MOSFETs. Continuous-time amplifiers find extensive applications in analog and mixed-signal systems. Considering the structural

simplicity, ease of design, and level of performance, the versatile amplifier family introduced should find practical applications in monolithic analog and mixed-signal systems. The charge injection effects of MOSFETs are problematic in many circuit designs employing MOSFET switches, including sample-and-hold circuits and data converters. The macromodel introduced, which is convenient to use, should be helpful for the further development of analog and mixed signal circuits such as high speed high resolution sample-and-hold circuits and data converters.

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